

Compal confidential

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_PM+ICH9-M core logic

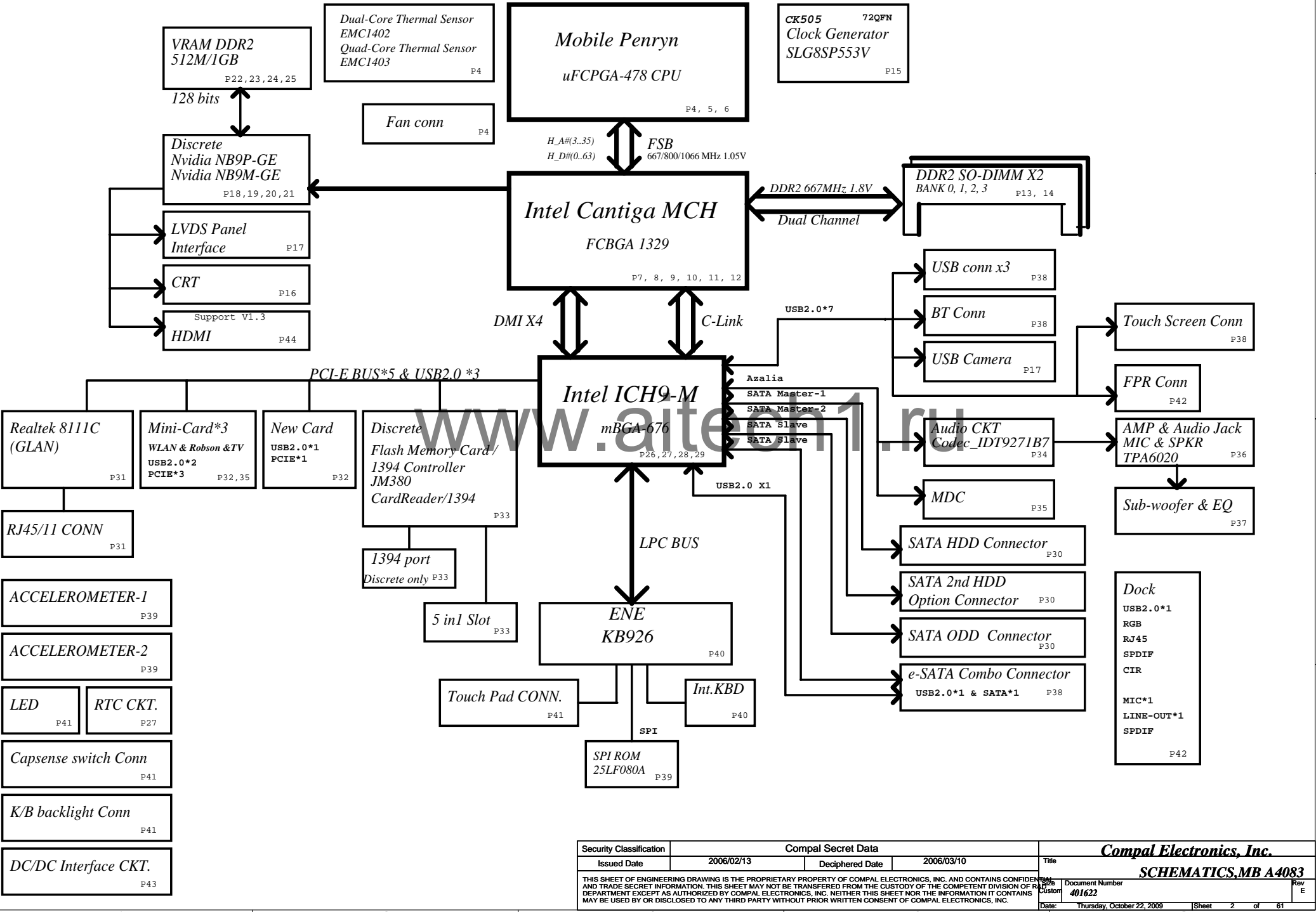
LA-4083P Vader Discrete (NB9P-GS,NB9M-GE)

2009-10-20 Rev 1.0

機 密	等級	硬體二部
	產出人員	
	產出日期	
	解密日期	

Security Classification	Compal Secret Data			Title	
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Montevina Consumer Discrete





power plane	State			
				+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
		+B	+5VALW +3VALW	+1.8V
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBus Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Sensor board
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X
DDC2_CLK DDC2_DATA	NB9M	X	X	X	X	X	X	X	V	X

USB
assignment:
USB-0 Right side
USB-1 Right side
USB-2 Left side(with ESATA)
USB-3 Dock
USB-4 Camera
USB-5 WLAN
USB-6 Bluetooth
USB-7 Finger Printer
USB-8 MiniCard(WWAN/TV)
USB-9 Express
USB-10 X
USB-11 X

PCIe
assignment:
PCIe-1 TV tuner/WWAN/Robeson
PCIe-2 X
PCIe-3 WLAN
PCIe-4 New Card
PCIe-5 Card
PCIe-6 GLAN (Marvell)

Symbol Note :
 : means Digital Ground
 : means Analog Ground

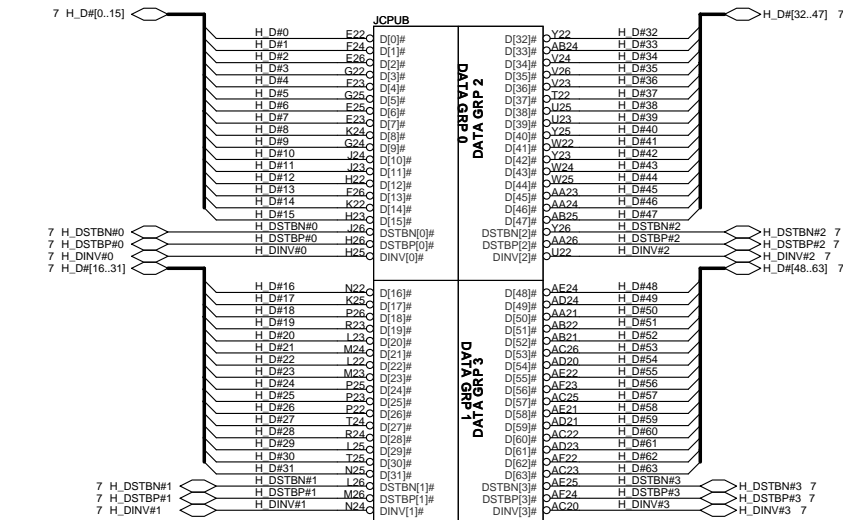
@ : means just reserve , no build
DEBUG@ : means just reserve for debug.

EC SM Bus1 address			EC SM Bus2 address		
Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X	CPU EMC1402	4CH	1001 1000b
24C16	A0H	1010 000X	VGA	4DH	1001 1010b
CAP BOARD -- Cypress	38H				
CAP BOARD -- ST	b0H				
G-sensor		0011 1001(read) 0011 1010(write)			

I2C / SMBUS ADDRESSING

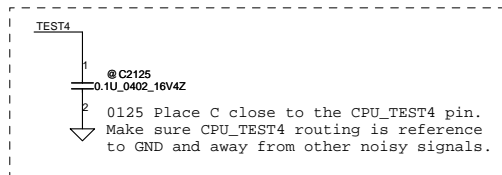
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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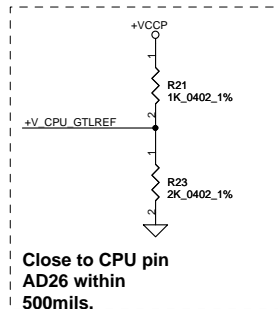


* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

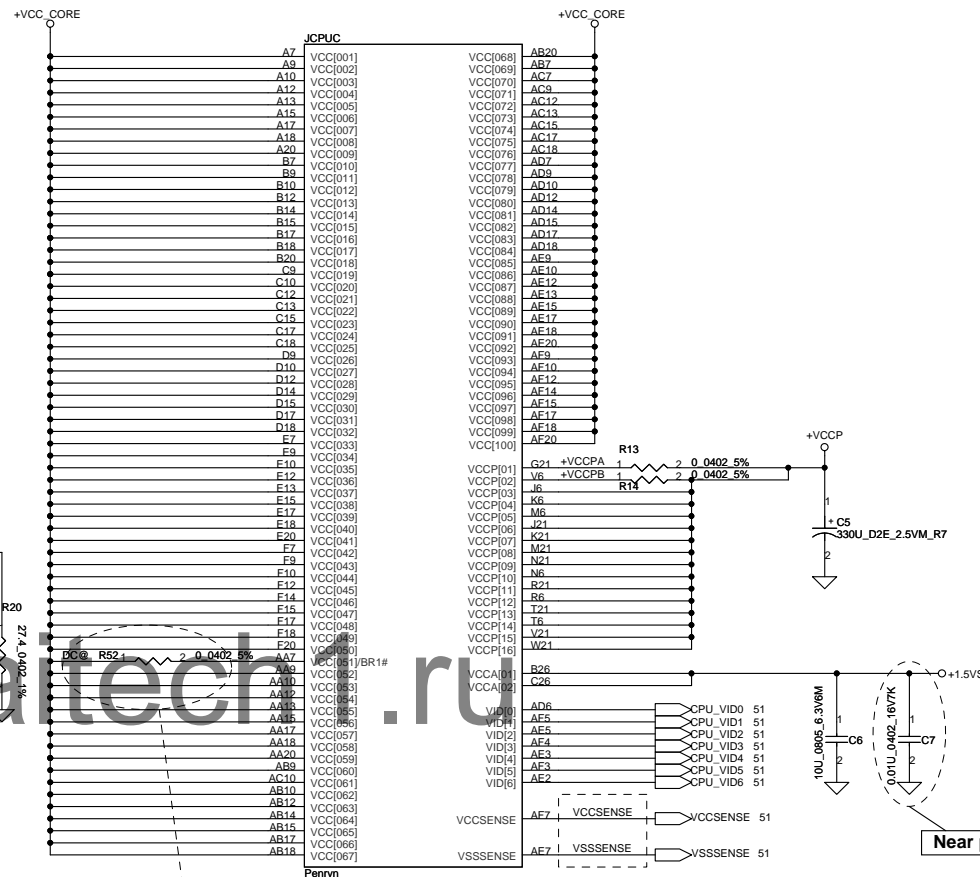
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

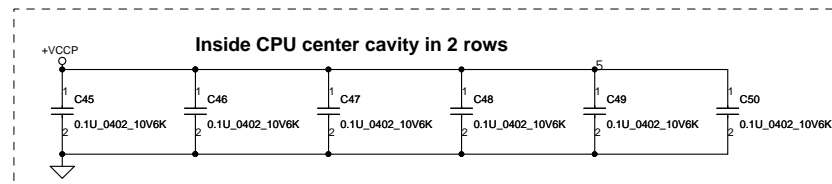
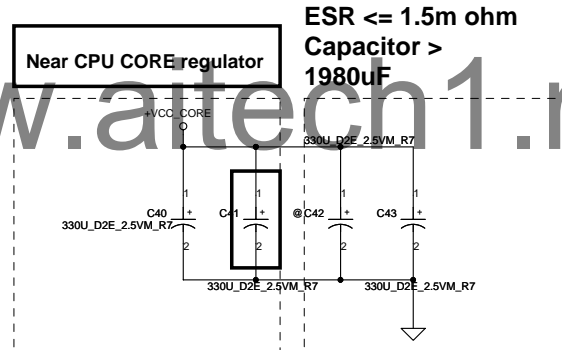
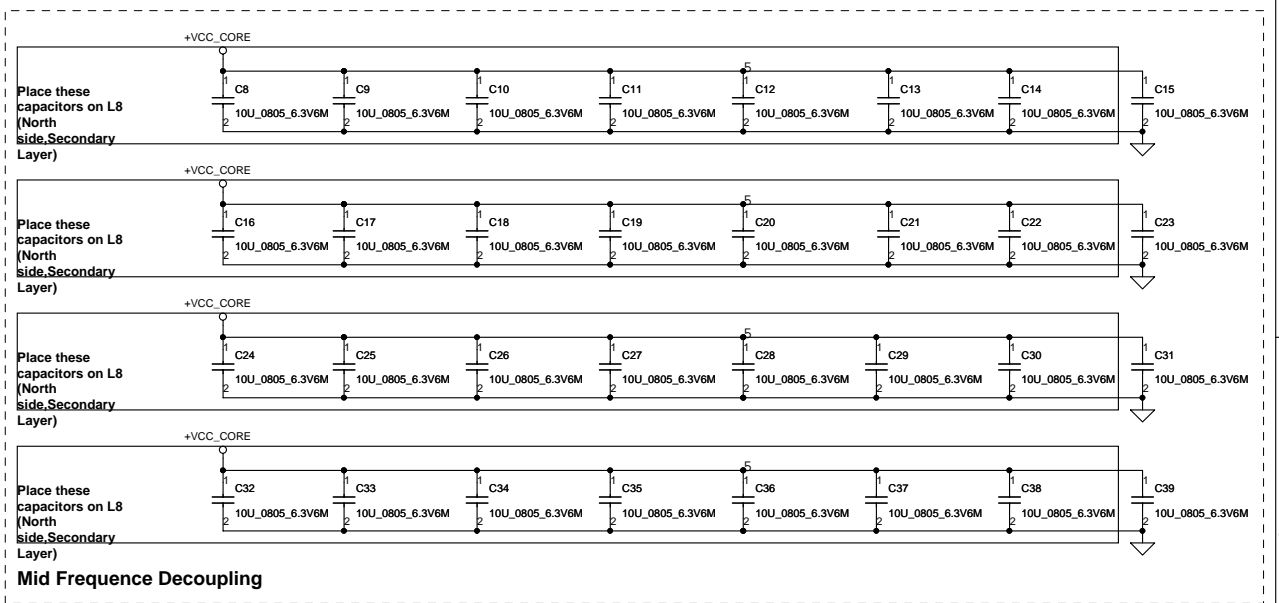
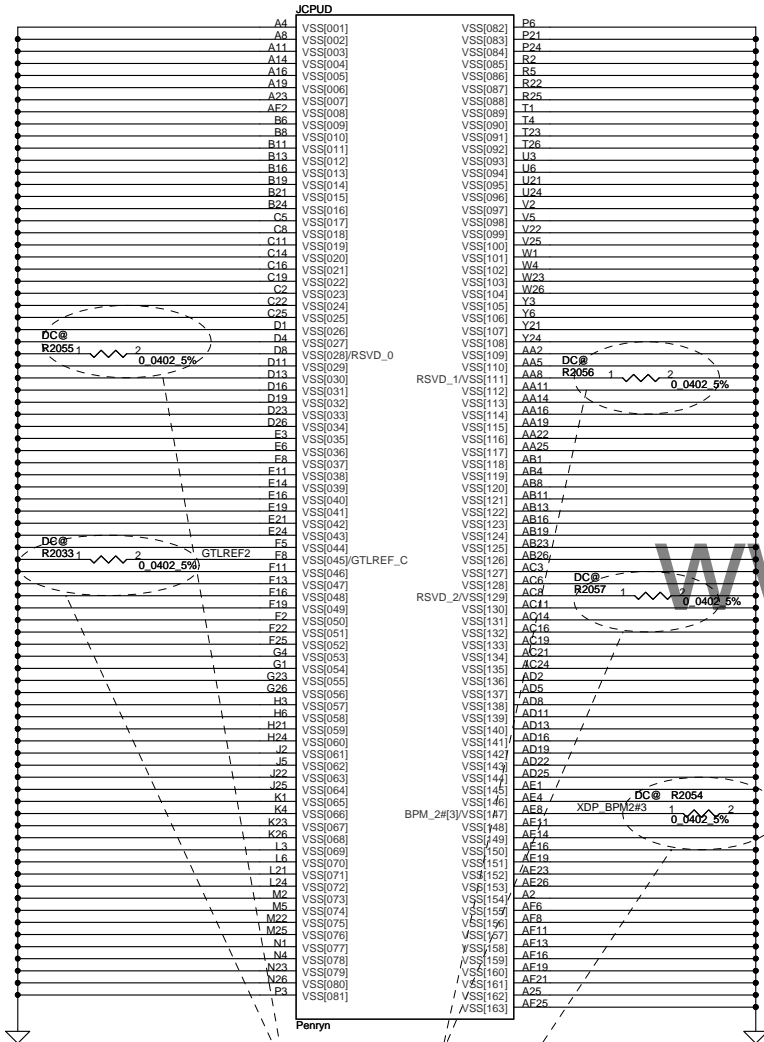


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.



1025 For Support Dual core and Quad core

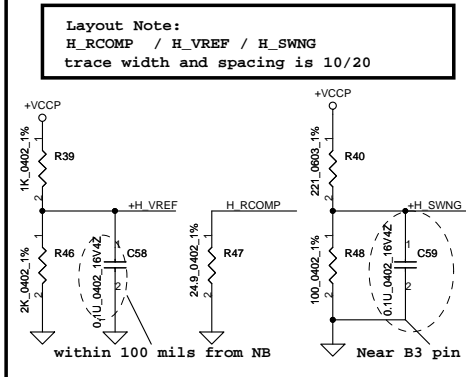




GTLREF2 → GTLREF2 4
XDP_BPM2#3 → XDP_BPM2#3 4

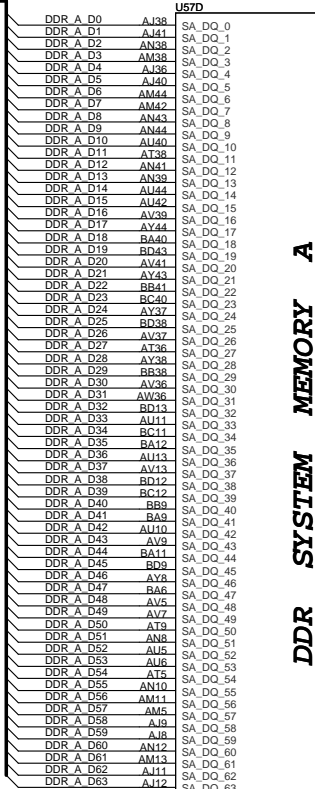
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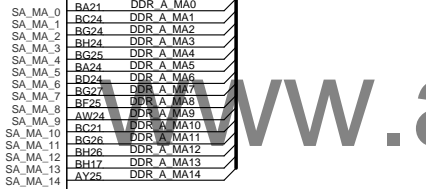
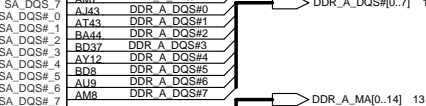
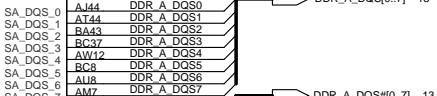
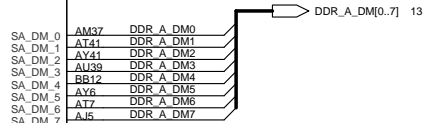
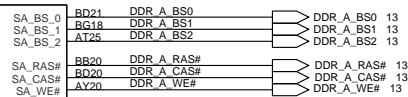
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13 DDR_A_D[0..63]

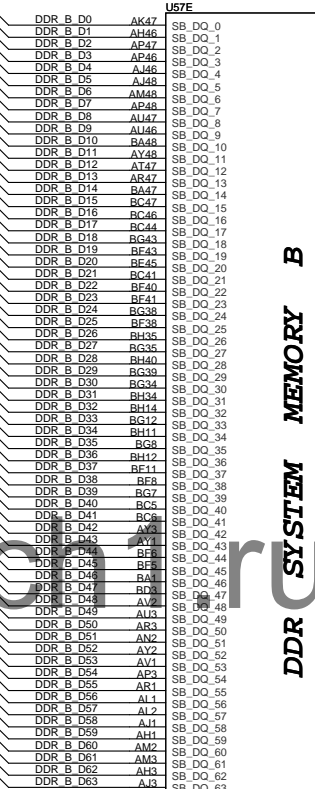


DDR SYSTEM MEMORY A

CANTIGA ES_FCBGA1329

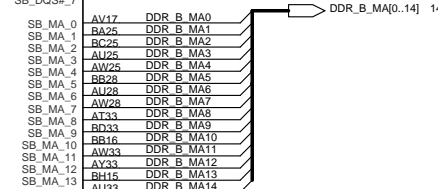
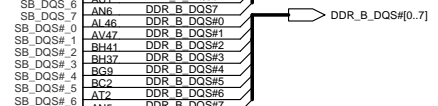
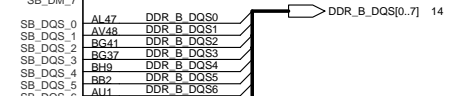
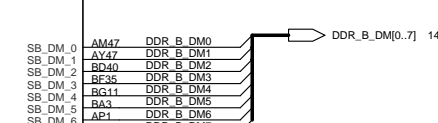
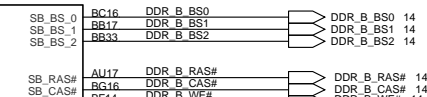


14 DDR_B_D[0..63]



DDR SYSTEM MEMORY B

CANTIGA ES_FCBGA1329



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U57G 3000mA

+1.8V

C158 330uF 4V

10uF 0.005 10V

10uF 0.005 10V

10uF 0.002 16V

C159

C160

C161

0317 change value

AP33 VCC_SM

AN33 VCC_SM

BH32 VCC_SM

PG32 VCC_SM

RB32 VCC_SM

BD32 VCC_SM

RC32 VCC_SM

BA32 VCC_SM

AY32 VCC_SM

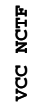
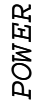
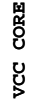
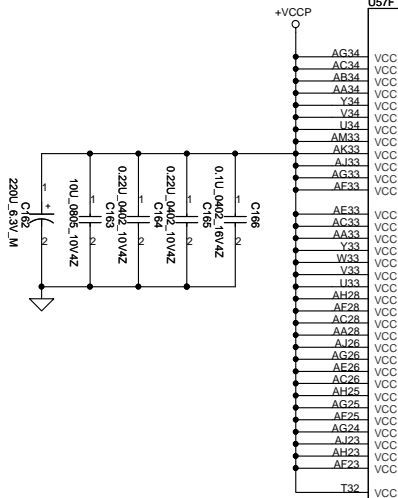
AW32 VCC_SM

AV32 VCC_SM

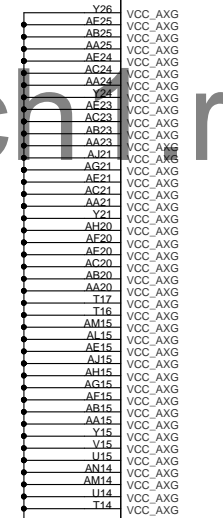
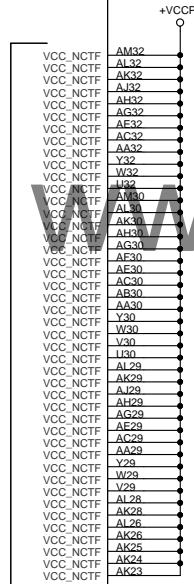
AU32 VCC_SM

AT32 VCC_SM

AR32 VCC_SM

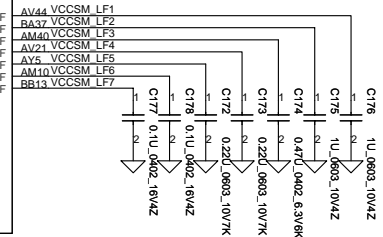
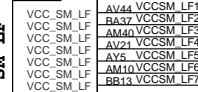


CANTIGA ES_FCBGA1329



VCC GEX

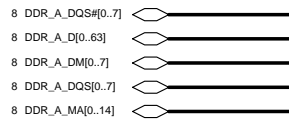
VCC SM T.F



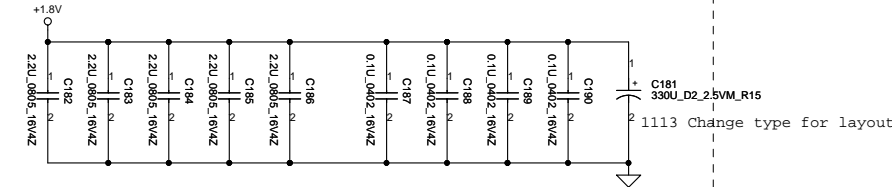
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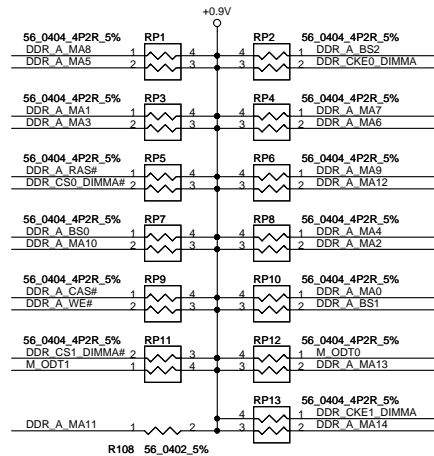
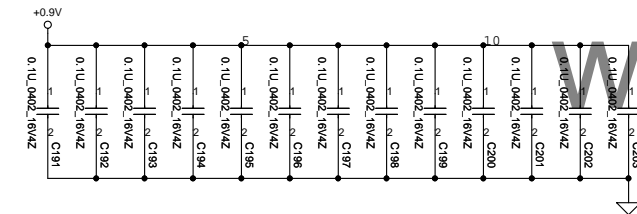
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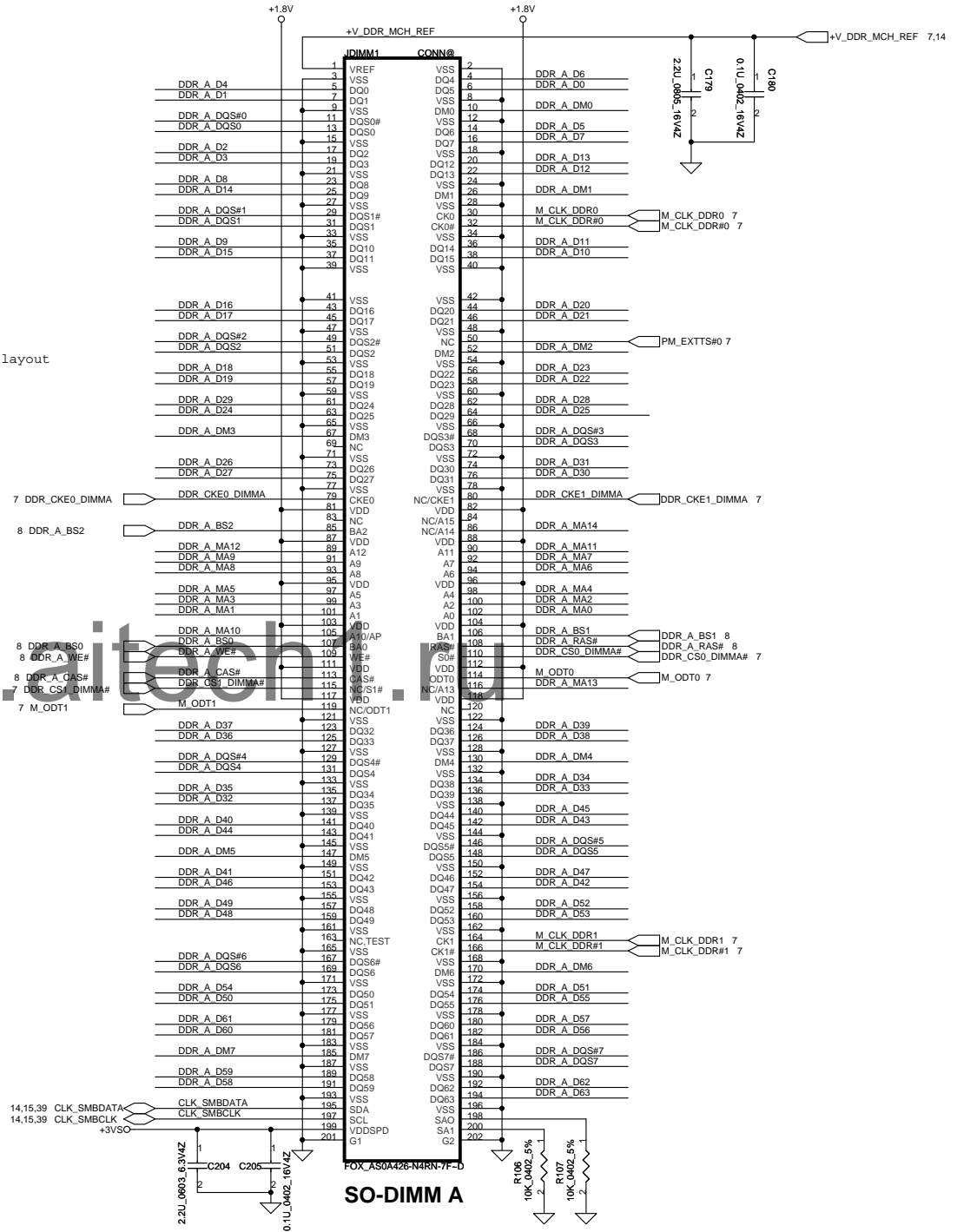
Layout Note:
Place near
JP3



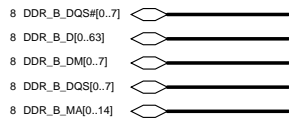
Layout Note:
Place one cap close to every
2 pullup
resistors terminated to +0.9VS



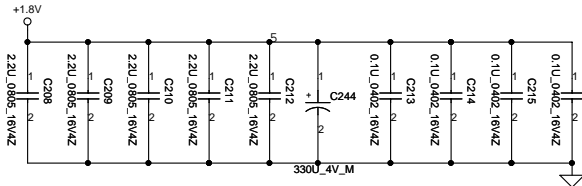
Layout Note:
Place these resistor
closely JP3,all
trace length Max=1.5\"/>



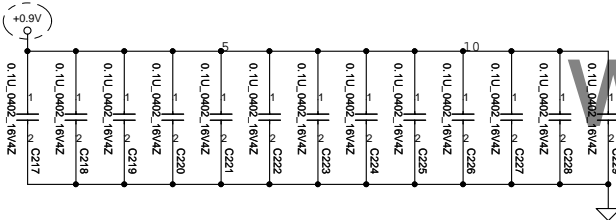
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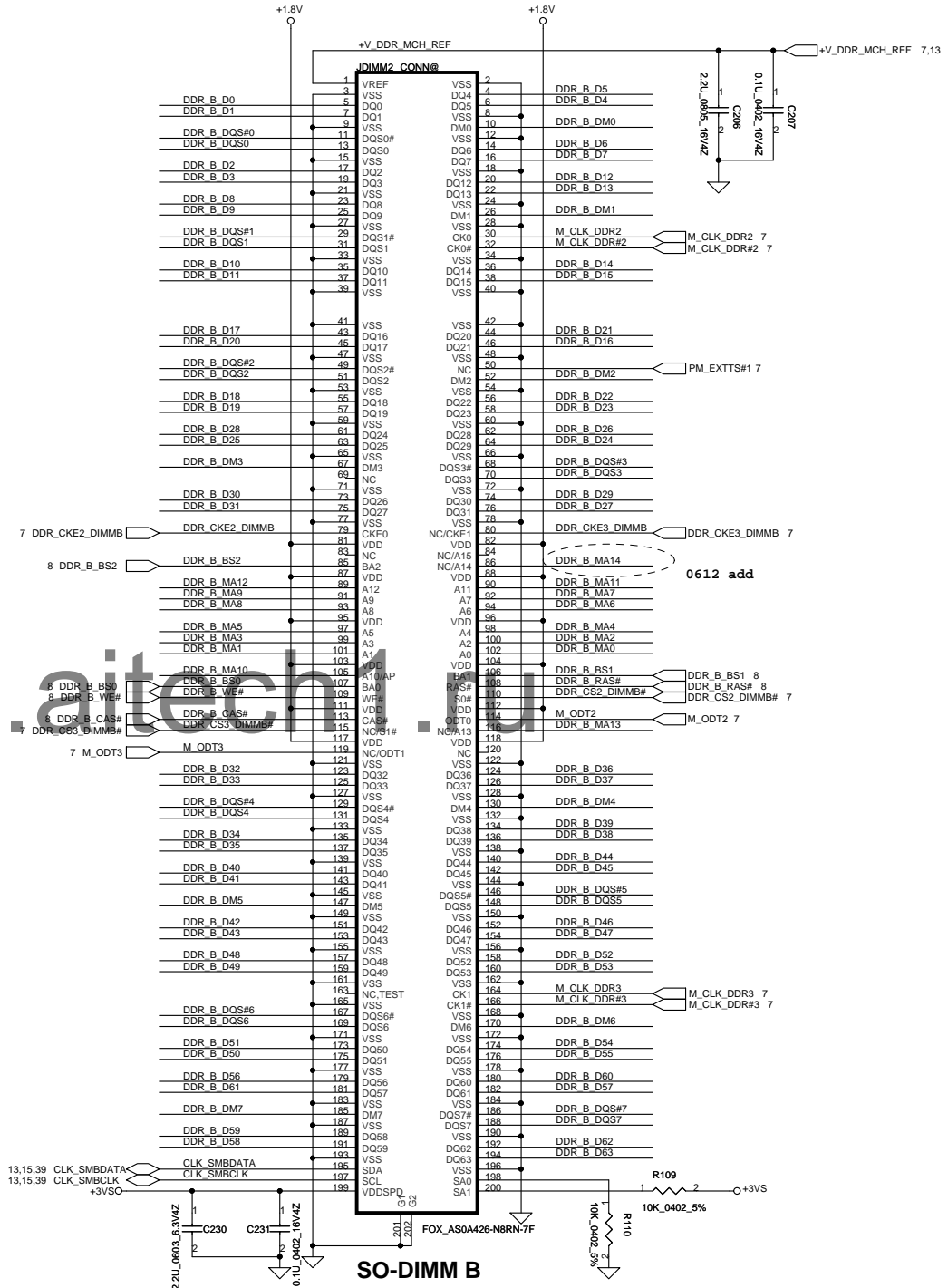
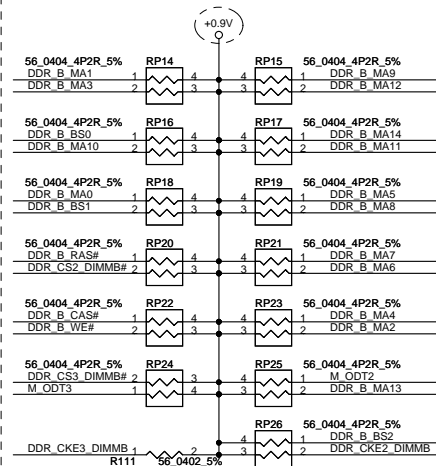
Layout Note:
Place near
JP10



Layout Note:
Place one cap close to every
2 pullup
resistors terminated to +0.9VS

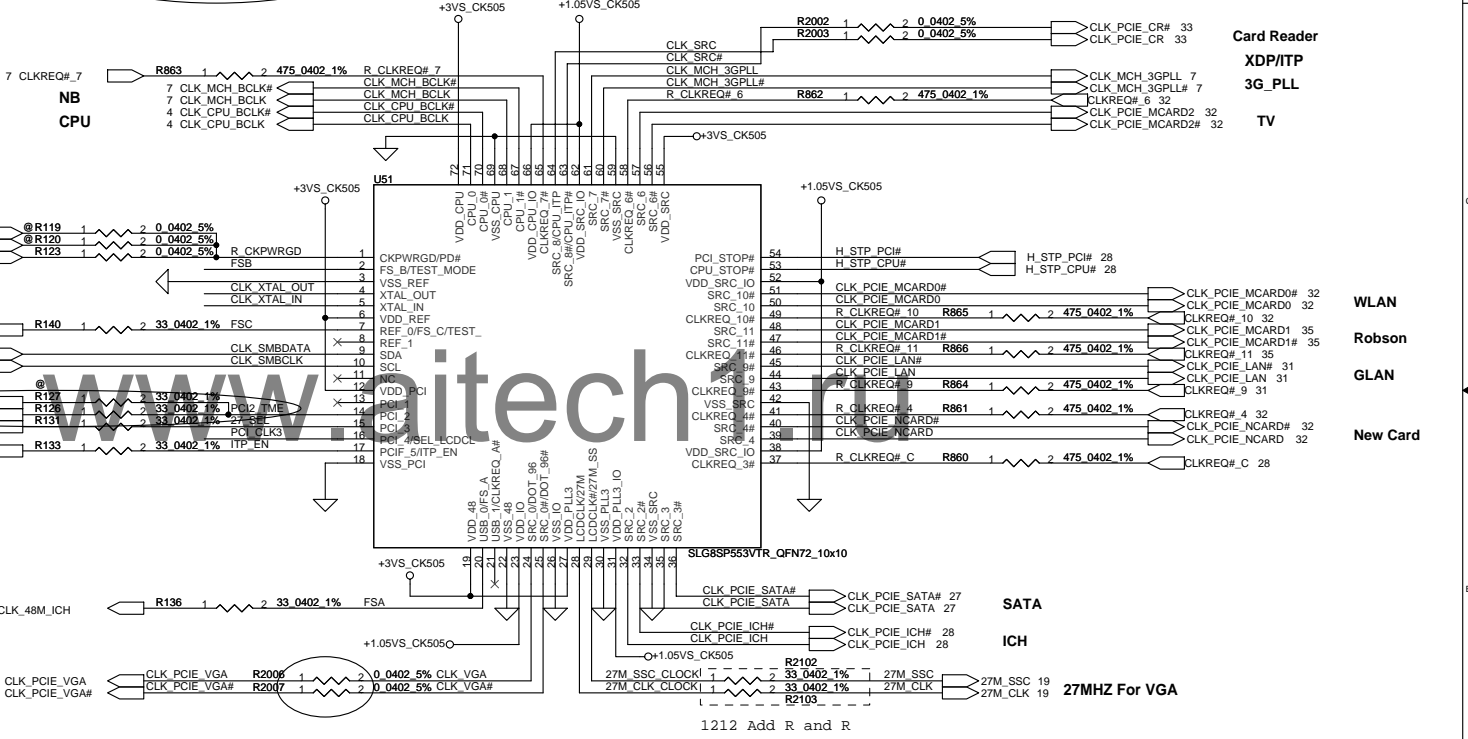
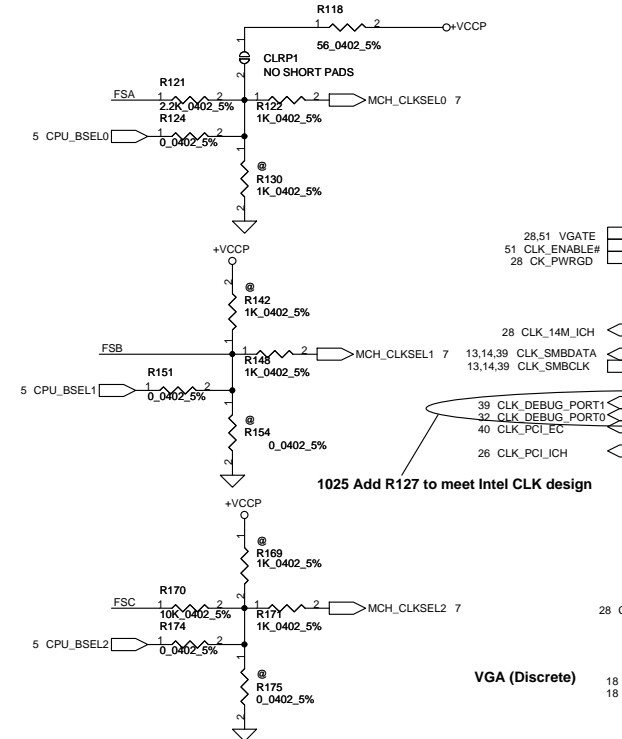
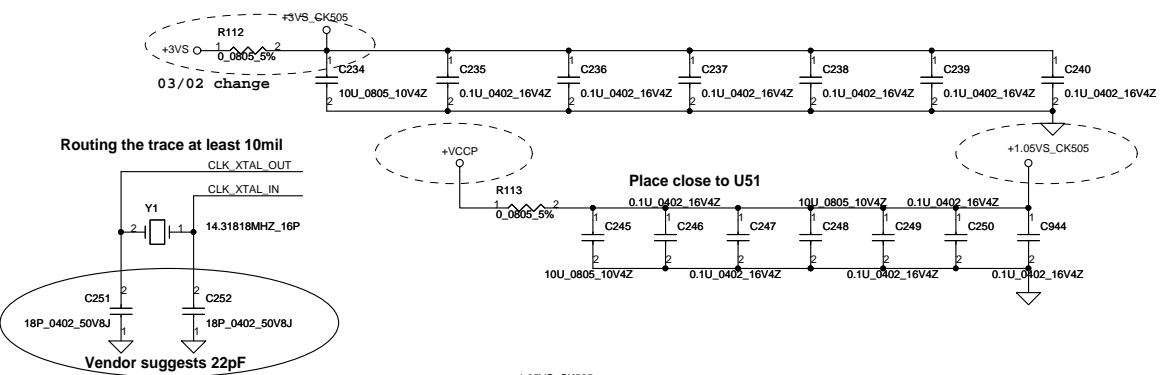


Layout Note:
Place these resistor
closely JP3, all
trace length Max=1.5"

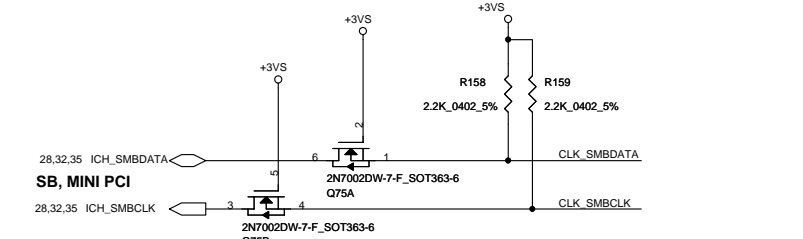


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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
PCI_CLK3	0 = Enable DOT96 & SRC1(UMA) 1 = Enable SRC0 & 27MHz(DIS)



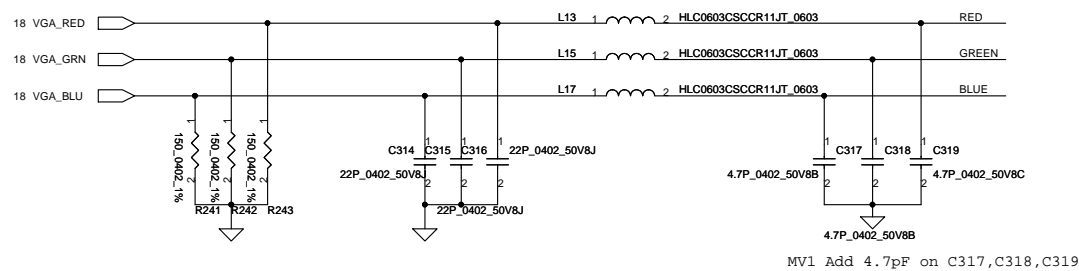
@ C232	5P_0402_50V8C	1	CLK_48M_ICH
@ C233	4.7P_0402_50V8C	2	CLK_14M_ICH
@ C241	4.7P_0402_50V8C	2	CLK_PCI_ICH
@ C242	4.7P_0402_50V8C	2	CLK_PCI_EC
@ C243	5P_0402_50V8C	2	CLK_DEBUG_PORT0

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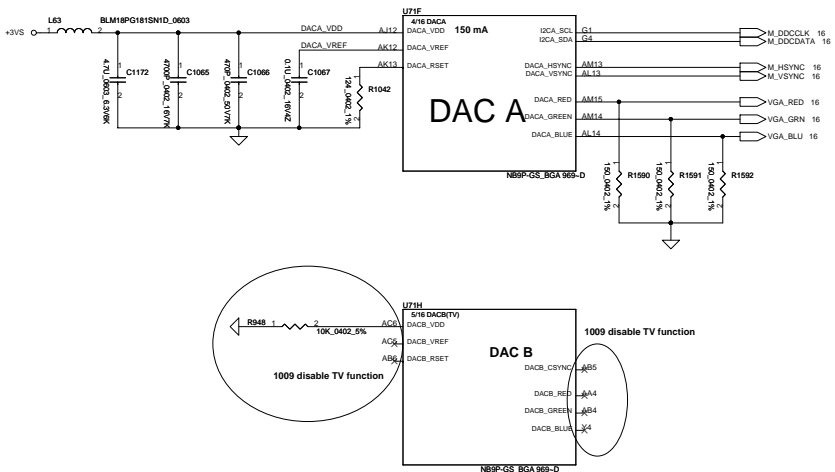
CRT Termination/EMI Filter

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

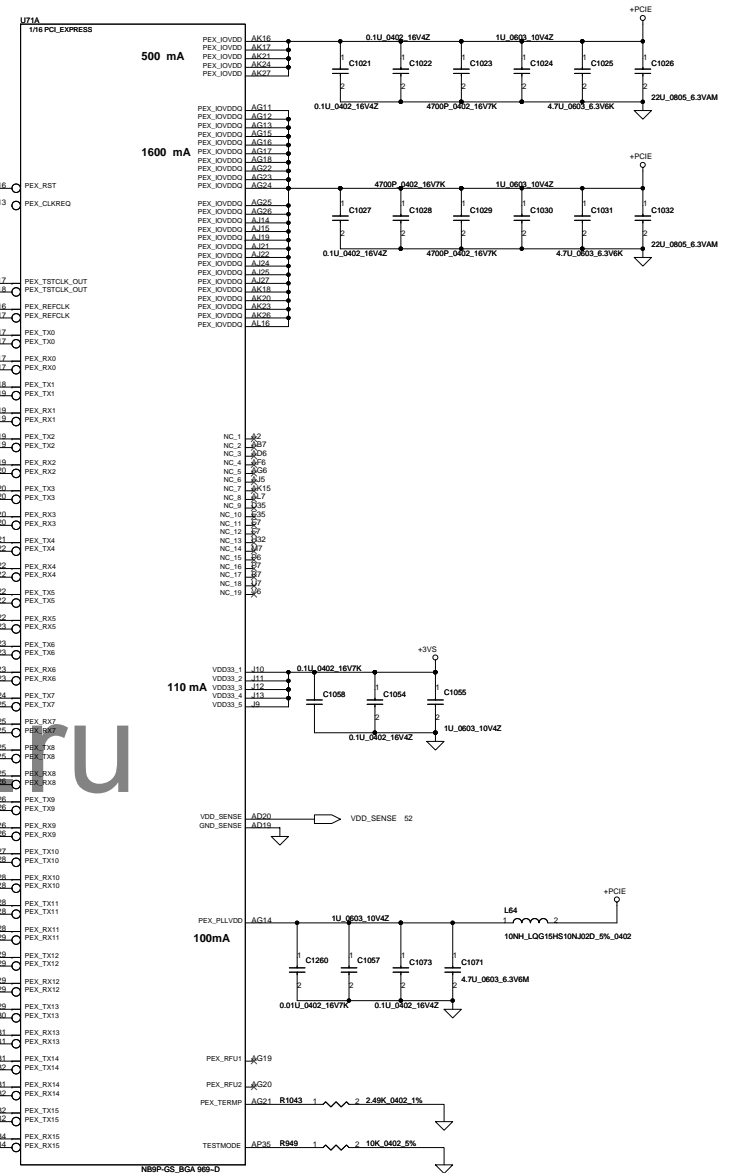




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				Document Number	E
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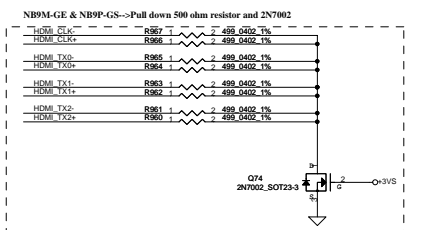
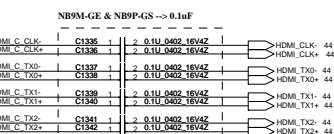
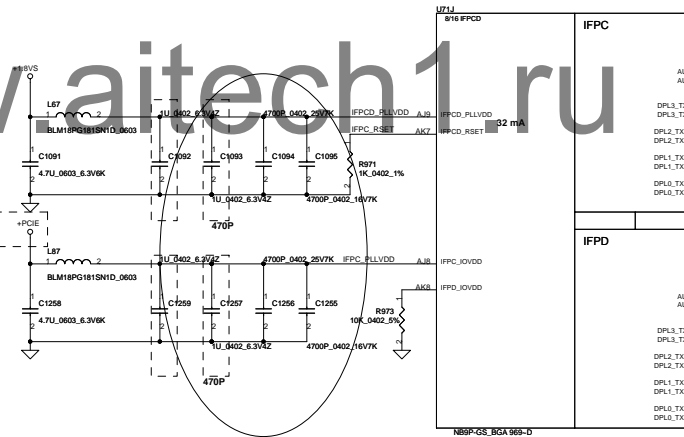
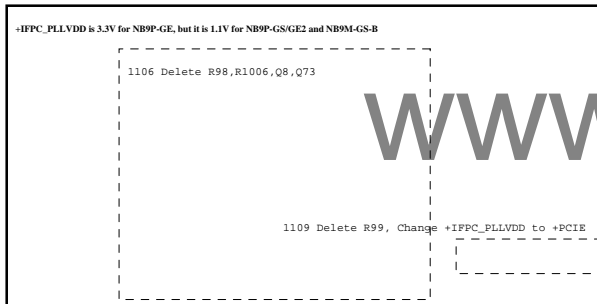
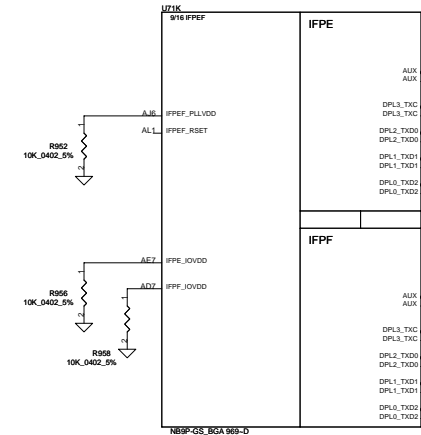
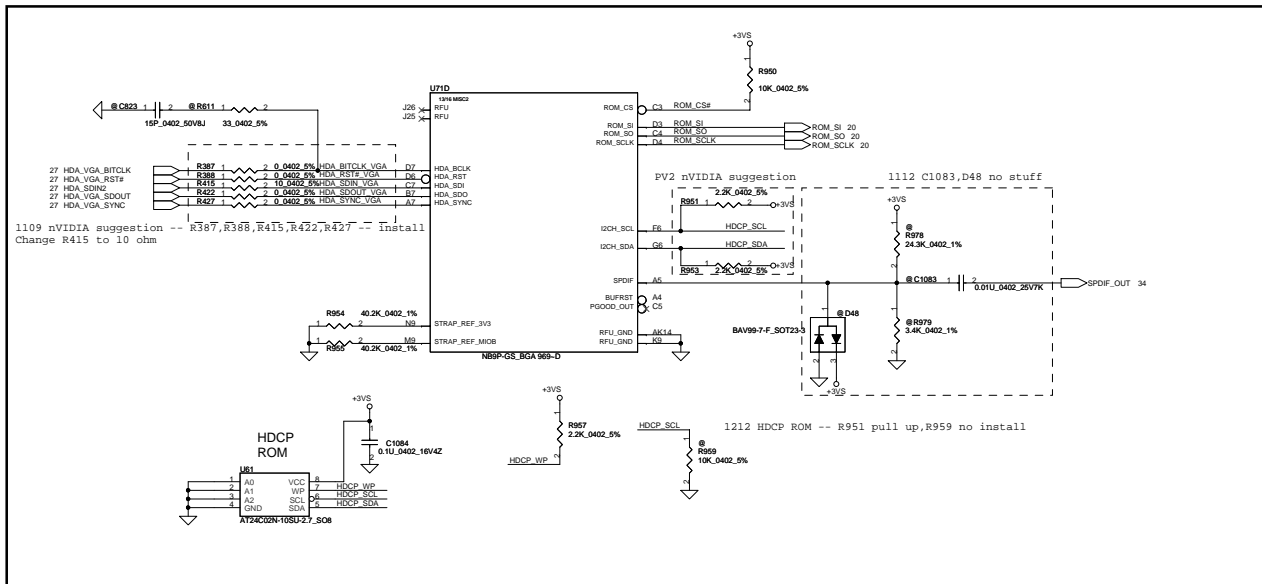
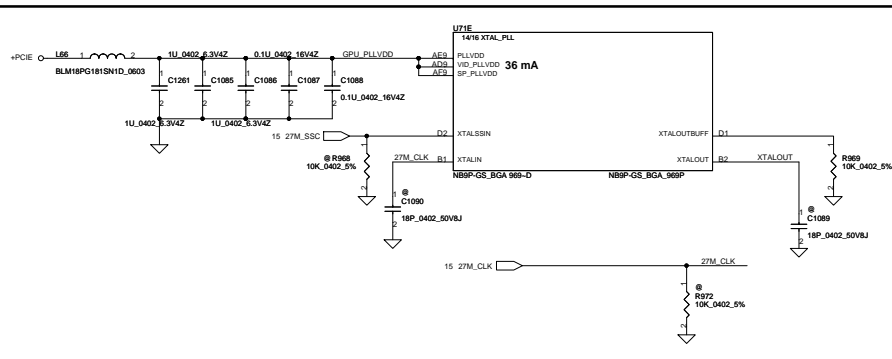
The schematic diagram illustrates the power supply section of the NBP-GS BGA 960-D. It features two voltage regulators, U716 (FPAB) and U718 (FPAB), both configured as 32 mA and 145 mA regulators. The input to both regulators is +1.8V_{SS}. The output of U716 is 32 mA, and the output of U718 is 145 mA. The regulators are connected to the LVDS_B+ and LVDS_B- pins of the BGA. The schematic includes various components such as capacitors (C1018, C1033, C1034, C1035, C1036, C1037, C1038), inductors (L61, L62), and resistors (R1044). The regulators are also connected to the LVDS_B+ and LVDS_B- pins of the BGA. The schematic is labeled with component values and pin numbers.



26.31,32,33.35 PLT_RST

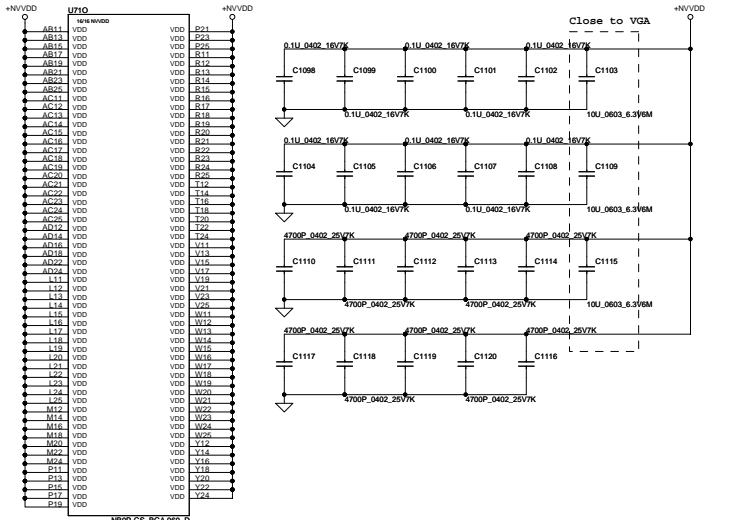


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			Date 2006-03-10	Rev 01

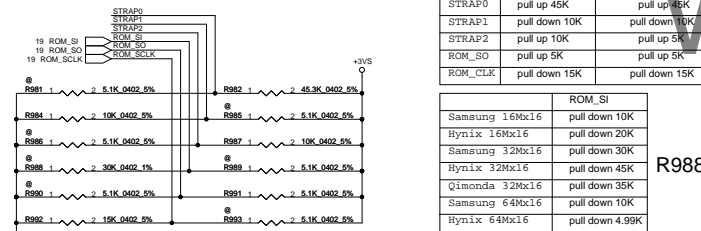


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Date: 2006/03/10 09:20:00			100000	10

VGA Core power

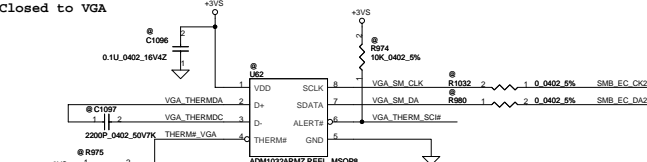


MULTI LEVEL STRAPS For NB9M-Gx (64bit)
NB9P-GS and NB9P-GE2 is as same as NB9M-GE-B

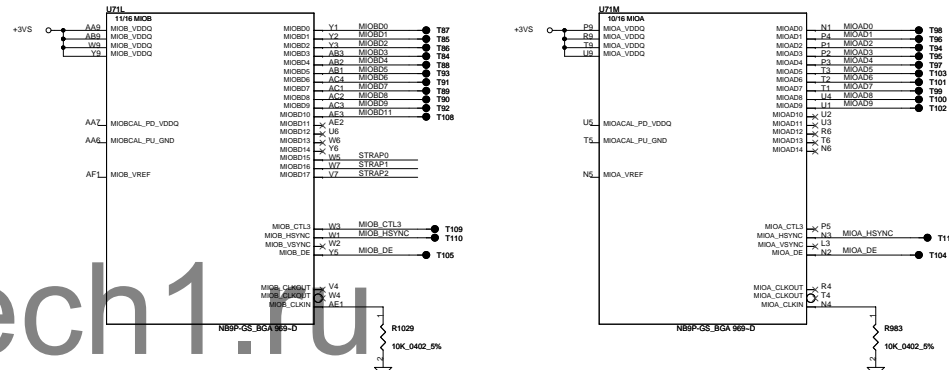
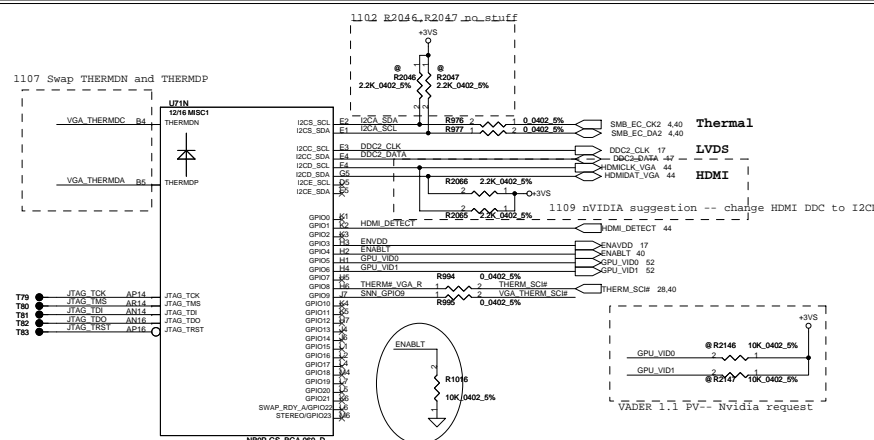


VGA Thermal Sensor ADM1032ARMZ

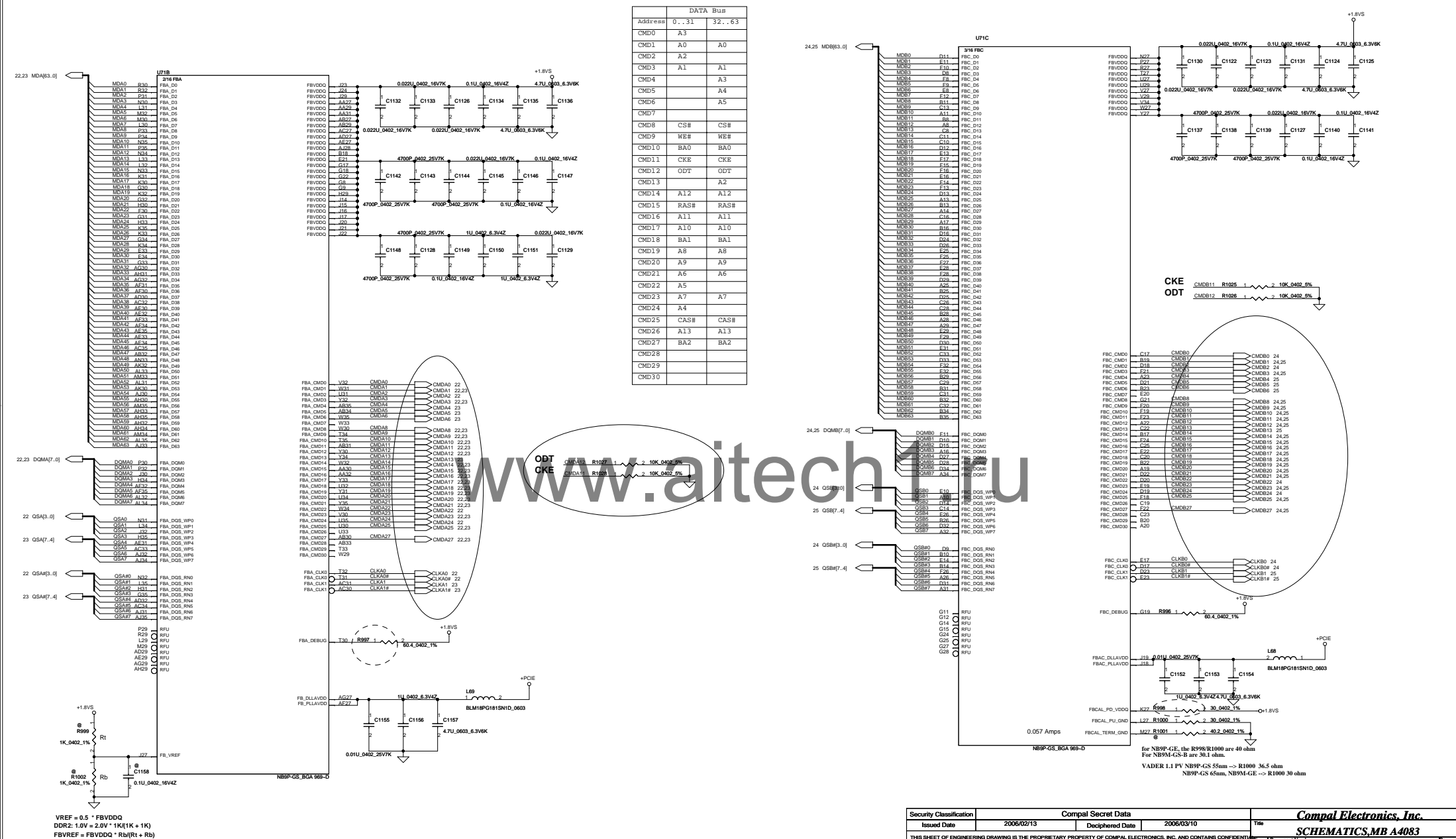
Closed to VGA



GPI0	I/O	ACTIVE	USAGE
GPI00	IN	N/A	Primary DVI Hot-plug
GPI01	IN	N/A	2nd DVI Hot-plug
GPI02	OUT	H	Panel Back-Light PWM
GPI03	OUT	H	Panel Power Enable
GPI04	OUT	H	Panel Back-Light Enable
GPI05	OUT	N/A	NVDD VID0
GPI06	OUT	N/A	NVDD VID1
GPI07	OUT	N/A	FBVDD VID0
GPI08	IN	L	Thermal Alert
GPI09	OUT	L	FAN PWM
GPI010	OUT	N/A	FBVref Select
GPI011	OUT	N/A	SLI SYNC0
GPI012	IN	N/A	AC Detect
GPI013	OUT	L	PS Control or HDMI_CEC
GPI014	OUT	H	PS Control



VRAM Interface



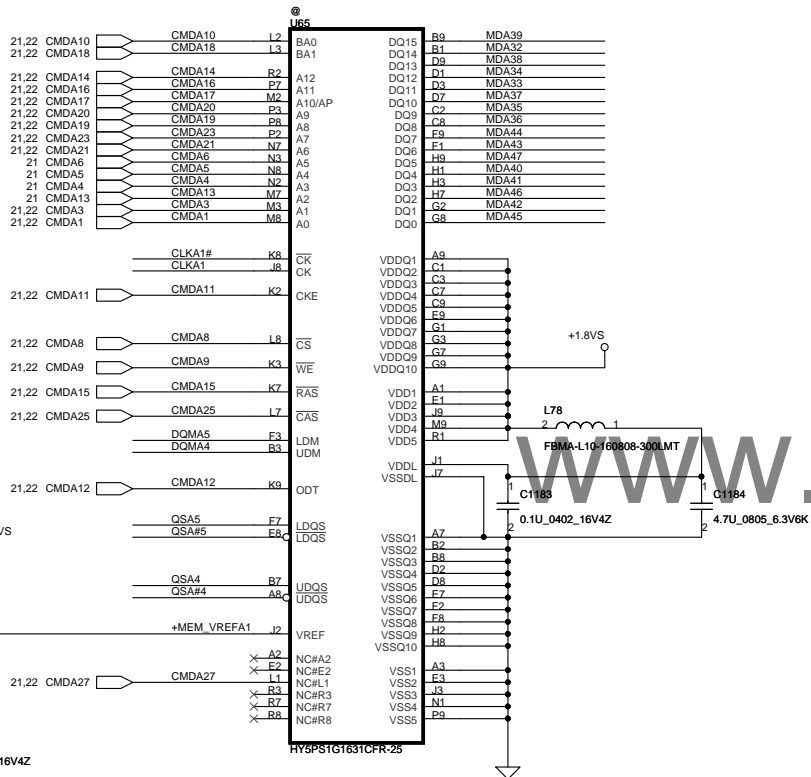
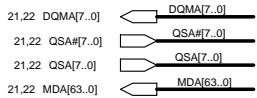
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			Date Tuesday, October 22, 2009	Sheet 91 of 61

64Mx16 DDR2 400MHz *4==>512MB

VRAM DDR2 chips (512MB & 1GB)

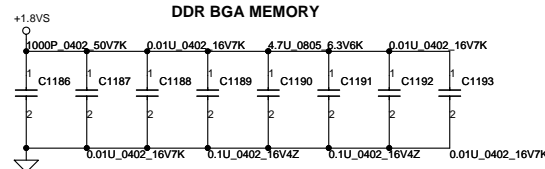
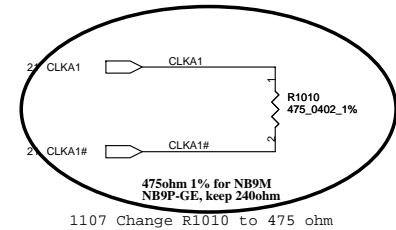
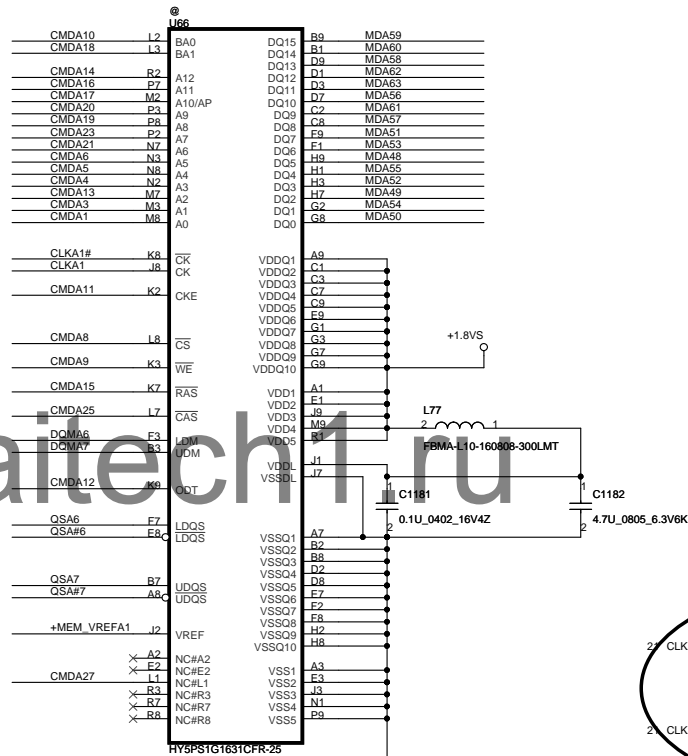
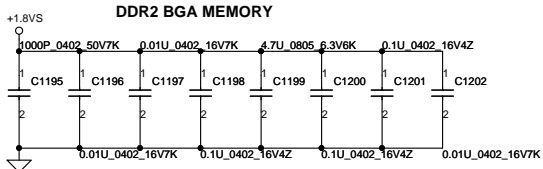
64Mx16 DDR2 400MHz *8==>1GB

64Mx16 DDR2 400MHz *4==>512MB



Vref= 0.5* 1.8V for NB9M, R1009=1K ohm

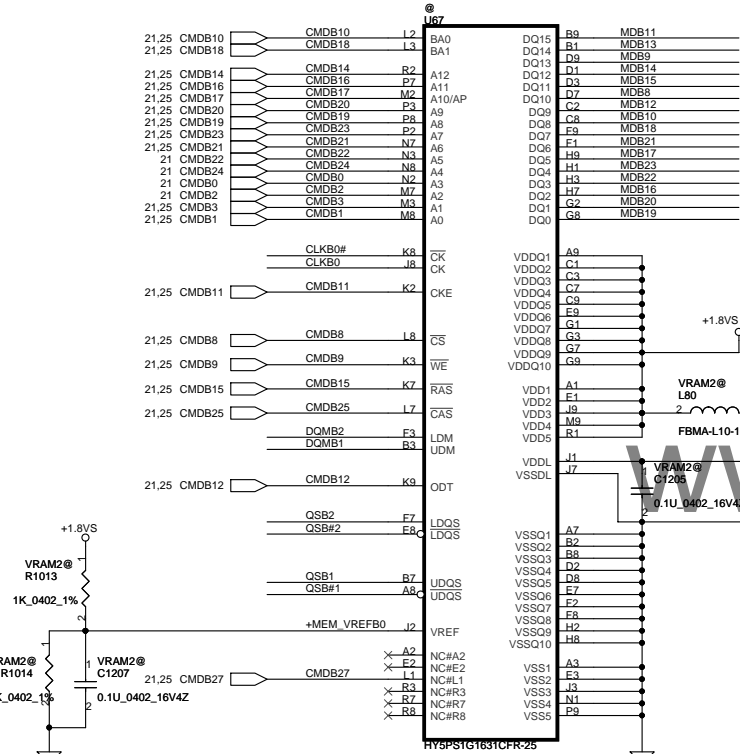
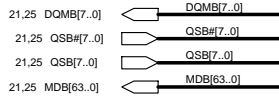
Vref= 0.5* 1.8V for NB9P-GS/GE2, R1009=1K ohm



Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

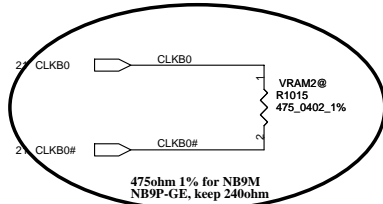
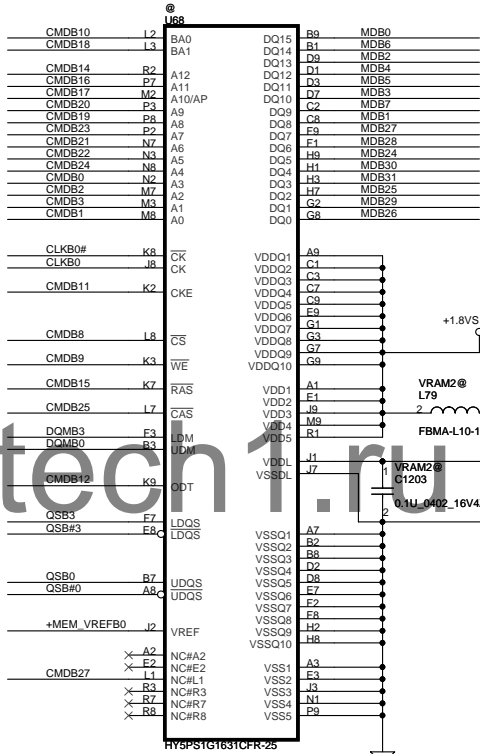
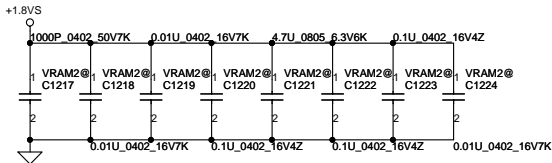
VRAM DDR2 chips (512MB & 1GB)

64Mx16 DDR2 400MHz *8==>1GB



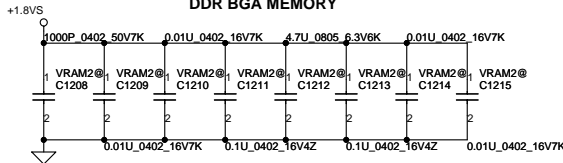
Vref= 0.5* 1.8V for NB9M, R1014=1K ohm
Vref= 0.5* 1.8V for NB9P-GS/GE2, R1014=1K ohm

DDR2 BGA MEMORY



1107 Change R1015 to 475 ohm

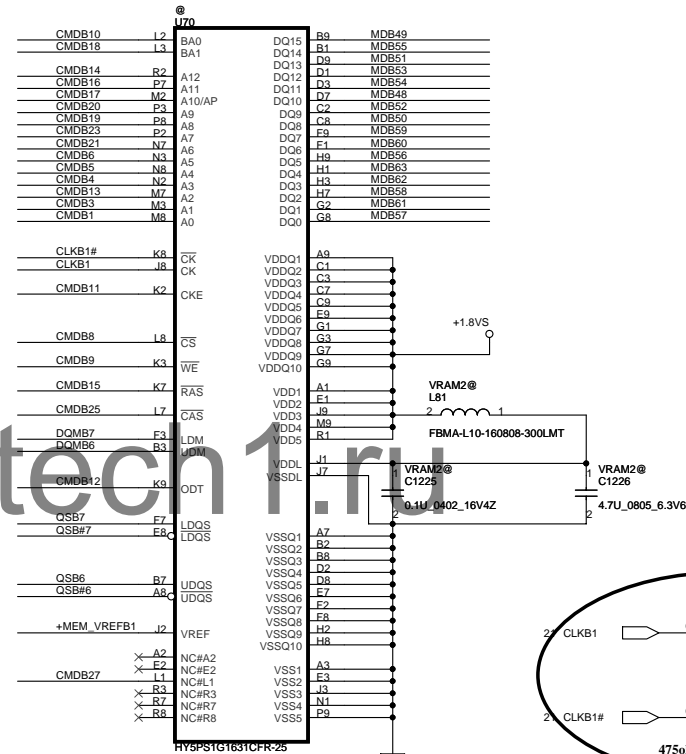
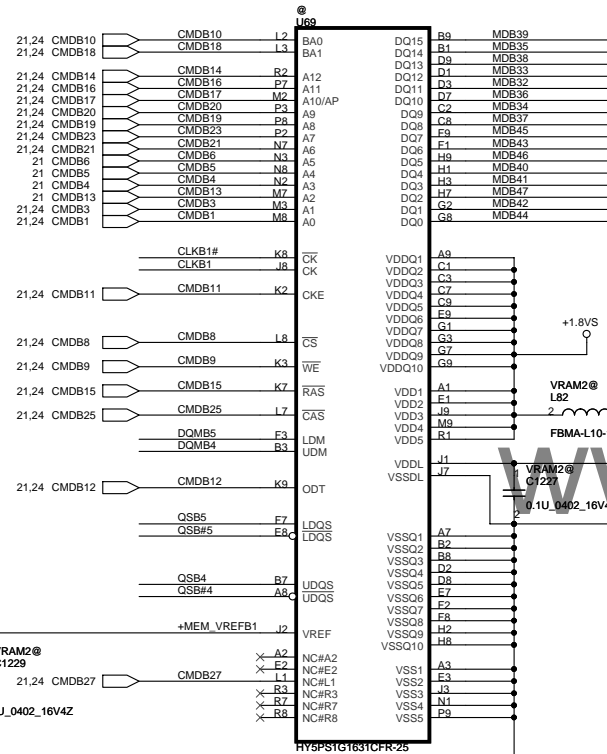
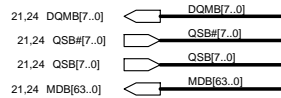
DDR2 BGA MEMORY



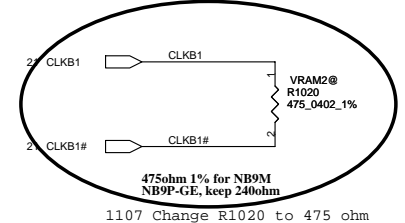
DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

VRAM DDR2 chips (512MB & 1GB)

64Mx16 DDR2 400MHz *8==>1GB



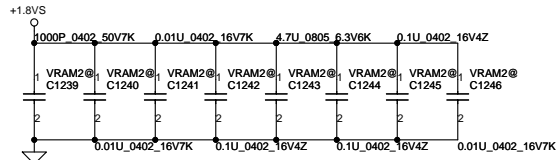
DATA Bus	
Address	0..31 32..63
CMD0	A3
CMD1	A0
CMD2	A2
CMD3	A1
CMD4	A3
CMD5	A4
CMD6	A5
CMD7	
CMD8	CS#
CMD9	WE#
CMD10	BA0
CMD11	CKE
CMD12	ODT
CMD13	A2
CMD14	A12
CMD15	RAS#
CMD16	A11
CMD17	A10
CMD18	BA1
CMD19	A8
CMD20	A9
CMD21	A6
CMD22	A5
CMD23	A7
CMD24	A4
CMD25	CAS#
CMD26	A13
CMD27	BA2
CMD28	
CMD29	
CMD30	



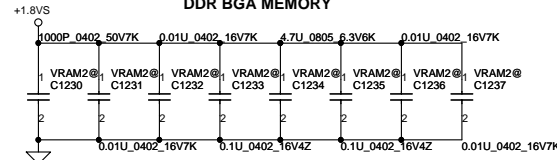
Vref= 0.5* 1.8V for NB9M, R1019=1K ohm

Vref= 0.5* 1.8V for NB9P-GS/GE2, R1019=1K ohm

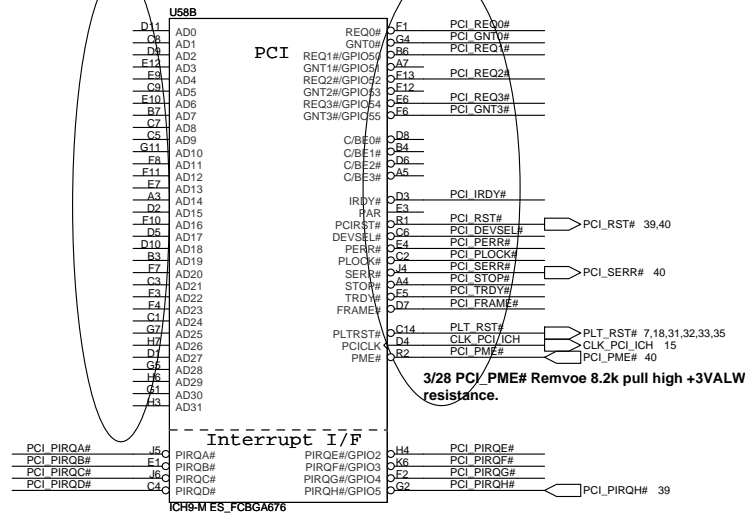
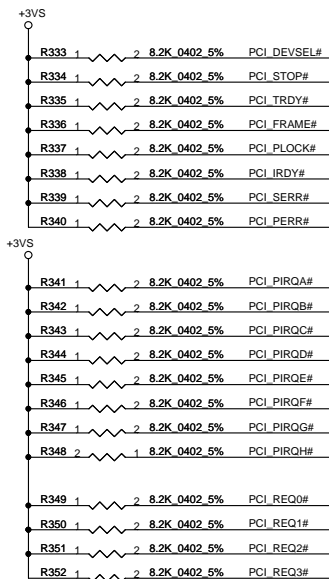
DDR2 BGA MEMORY



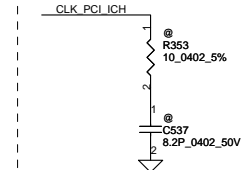
DDR BGA MEMORY



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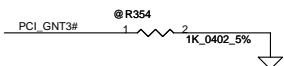
Place closely pin B10



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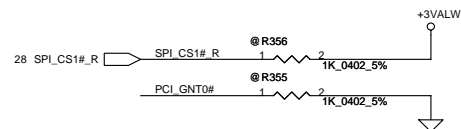
A16 swap override Strap

Low= A16 swap override Enable
High= Default *

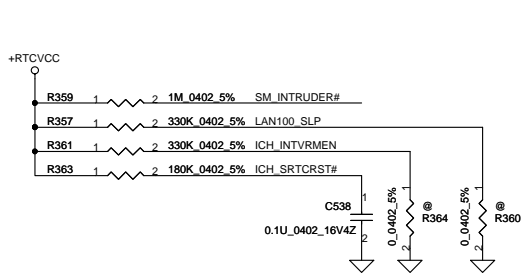


Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

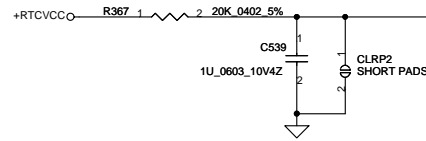
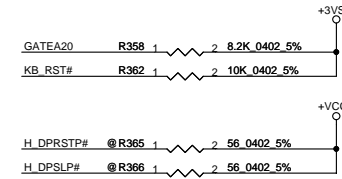
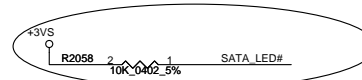


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Date: Thursday, October 22, 2009				Sheet	61



ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)		
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)	
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)		
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)	

1015 add pull up to meet Intel design

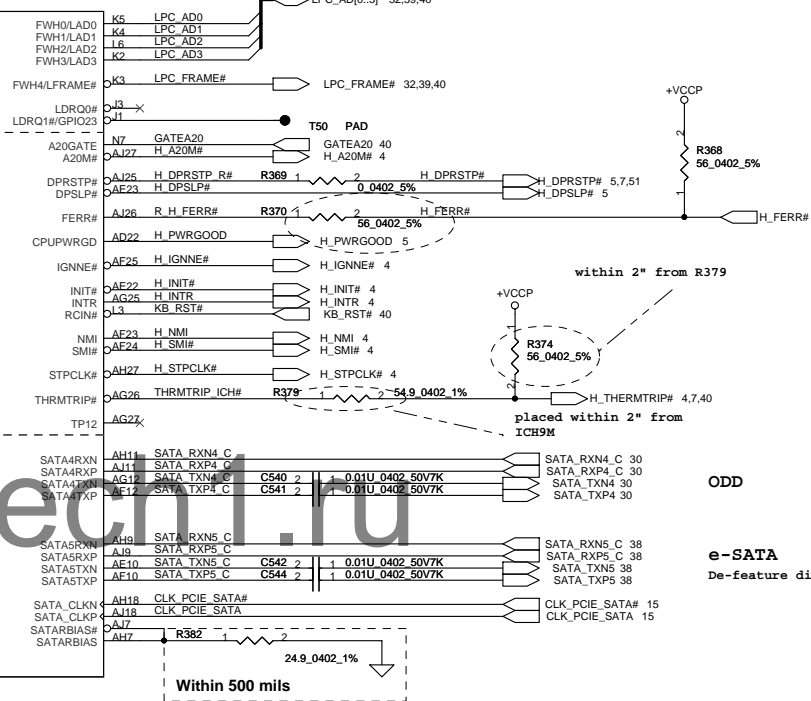


ICH_RTCX1	C23	RTCX1
ICH_RTCX2	C24	RTCX2
ICH_RTCSRST#	A25	RTCSRST#
ICH_SRTCSRST#	E20	SRTCSRST#
SM_INTRUDER#	C22	INTRUDER#
ICH_INTVRMEN	B22	INTVRMEN
LAN100_SLP	A22	LAN100_SLP
GLAN_CLK	E25	GLAN_CLK
LAN_RSTSYNC	C13	LAN_RSTSYNC
LAN_RXD0	E14	LAN_RXD0
LAN_RXD1	C13	LAN_RXD1
LAN_RXD2	D14	LAN_RXD2
LAN_TXD_0	D13	LAN_TXD_0
LAN_TXD_1	D12	LAN_TXD_1
LAN_TXD_2	E13	LAN_TXD_2
GPIO56	B10	GPIO56

HDA_BITCLK	A6	HDA_BIT_CLK
HDA_SYNC	A4	HDA_SYNC
HDA_RST#	A7	HDA_RST#
HDA_SDIN0	A4	HDA_SDIN0
HDA_SDIN1	A4	HDA_SDIN1
HDA_SDIN2	A3	HDA_SDIN2
HDA_SDIN3	A5	HDA_SDIN3
HDA_SDOUT	A5	HDA_SDOUT

SATA_LED#	A6	SATA_LED#
SATA_RXN0_C	A11	SATA_RXN0_C
SATA_RXP0_C	A16	SATA_RXP0_C
SATA_TXN0_C	A17	SATA_TXN0_C
SATA_TXP0_C	A17	SATA_TXP0_C
SATA_RXN1_C	A13	SATA_RXN1_C
SATA_RXP1_C	A13	SATA_RXP1_C
SATA_TXN1_C	A14	SATA_TXN1_C
SATA_TXP1_C	A14	SATA_TXP1_C

RTC
LPC
LAN / GLAN
CPU
HDA
SATA



ODD

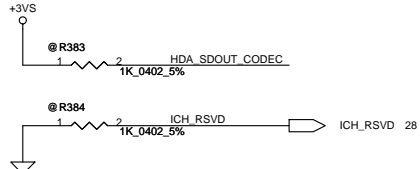
e-SATA
De-feature disable

P- HDD

S- HDD

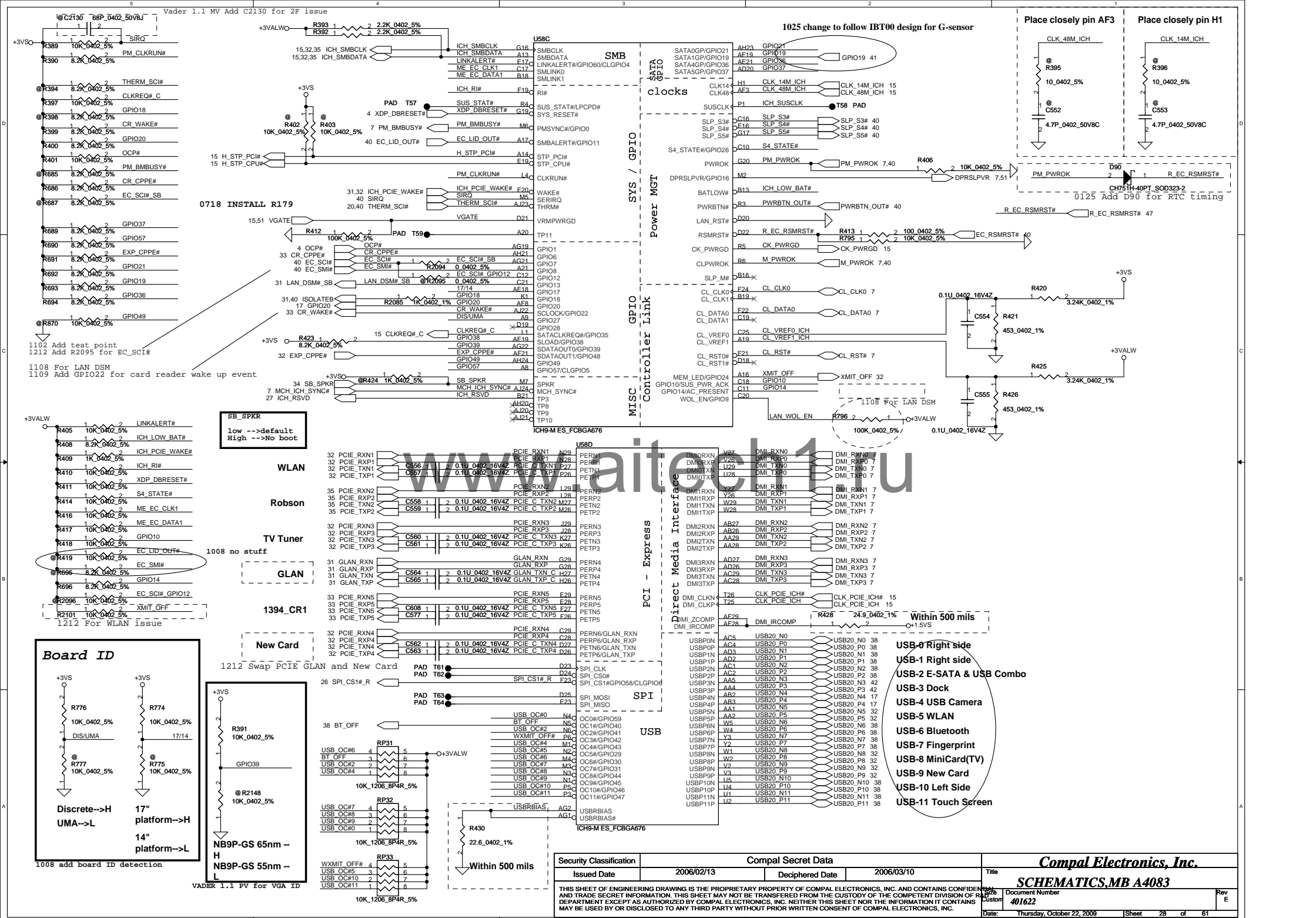
1212 Swap SATA1 and SATA4

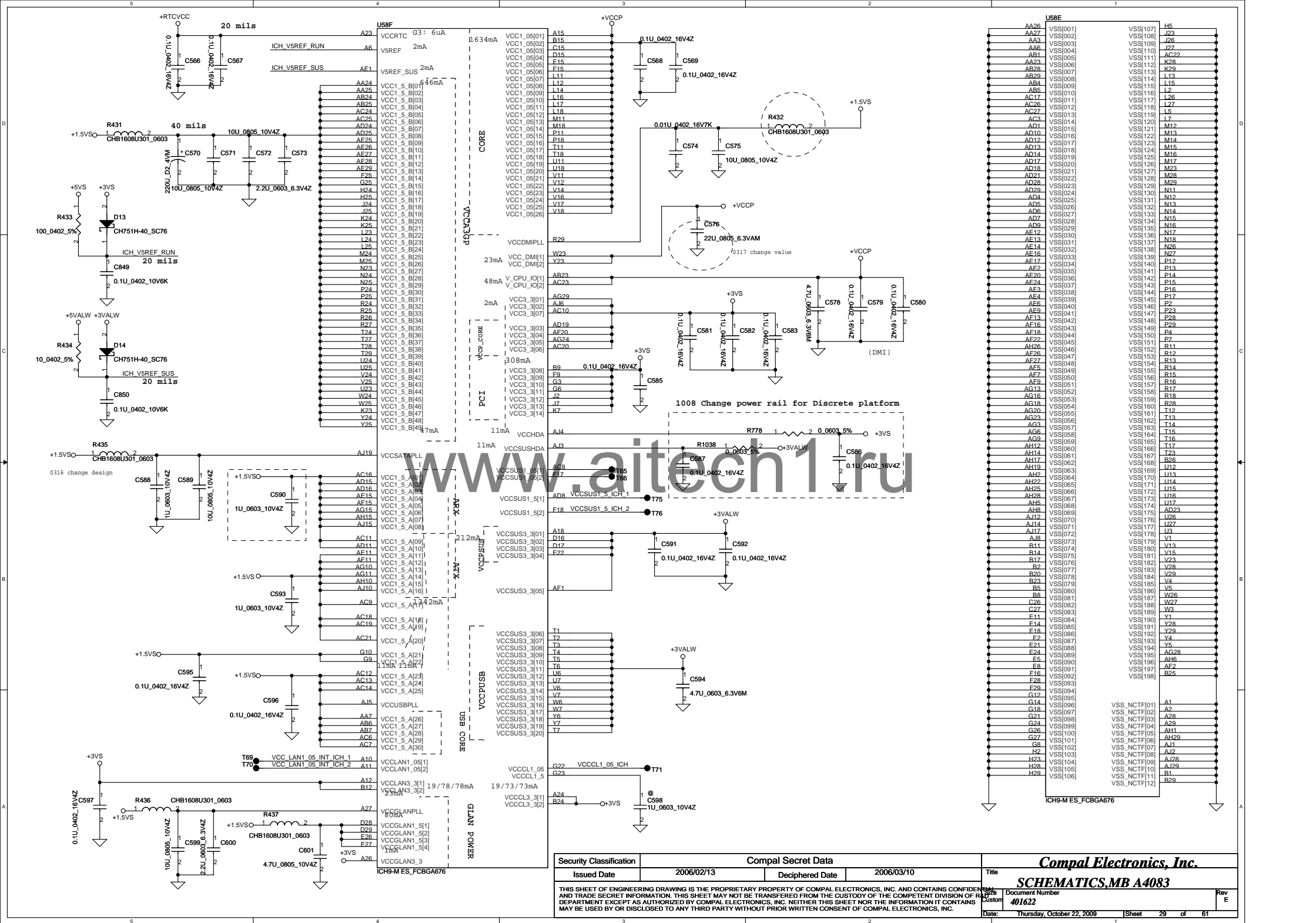
XOR CHAIN ENTRANCE STRAP:RSVD



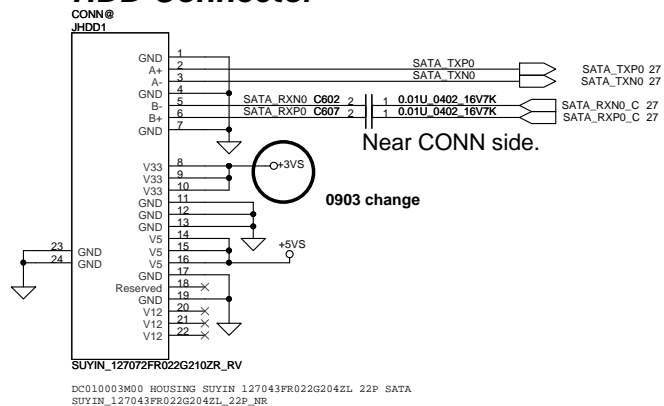
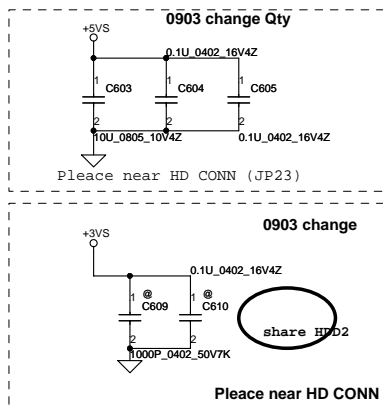
1008 add them for Intel suggestion

19 HDA_VGA_BITCLK	R439	33 0402 5%	HDA_BITCLK
35 HDA_BITCLK_MDC	R373	33 0402 5%	HDA_BITCLK
34 HDA_BITCLK_CODEC	R372	33 0402 5%	HDA_BITCLK
19 HDA_VGA_SYNC	R440	33 0402 5%	HDA_SYNC
35 HDA_SYNC_MDC	R375	33 0402 5%	HDA_SYNC
34 HDA_SYNC_CODEC	R376	33 0402 5%	HDA_SYNC
19 HDA_VGA_RST#	R442	33 0402 5%	HDA

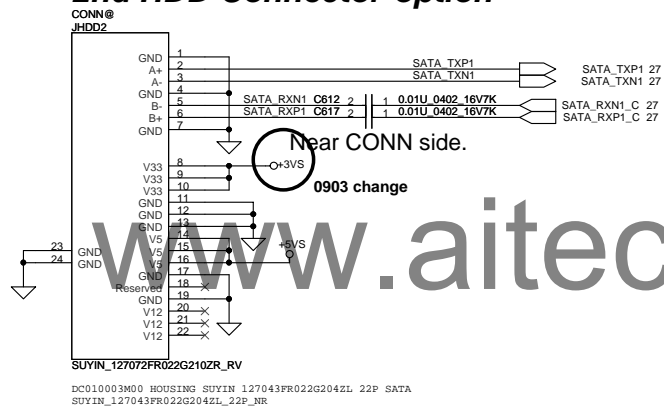
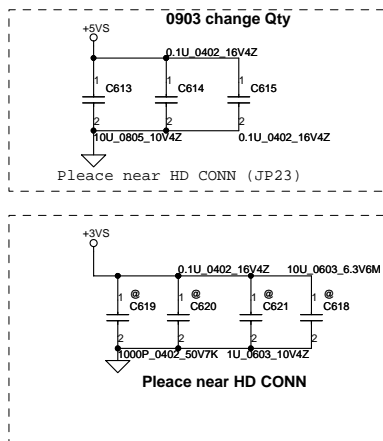




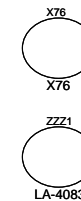
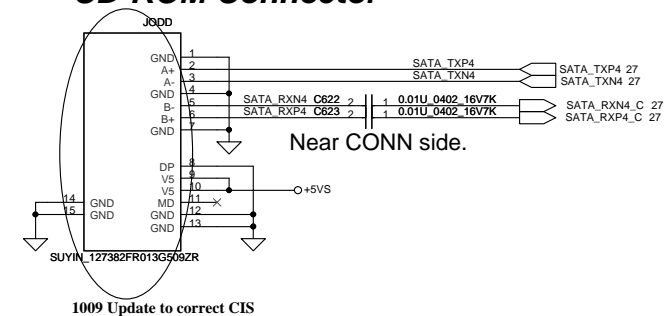
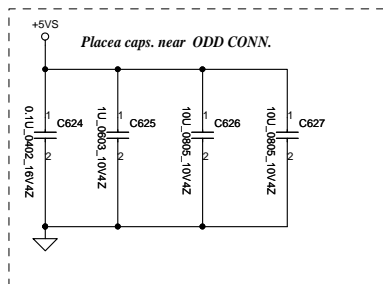
HDD Connector



2nd HDD Connector-option



CD-ROM Connector



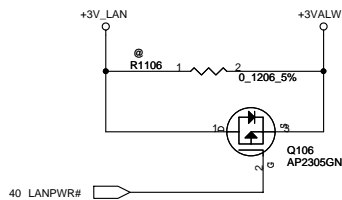
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Compal Electronics, Inc.

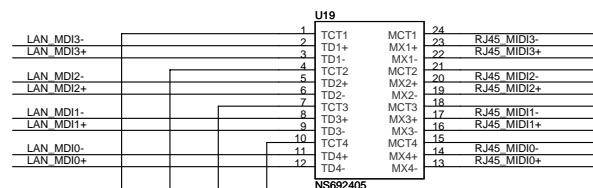
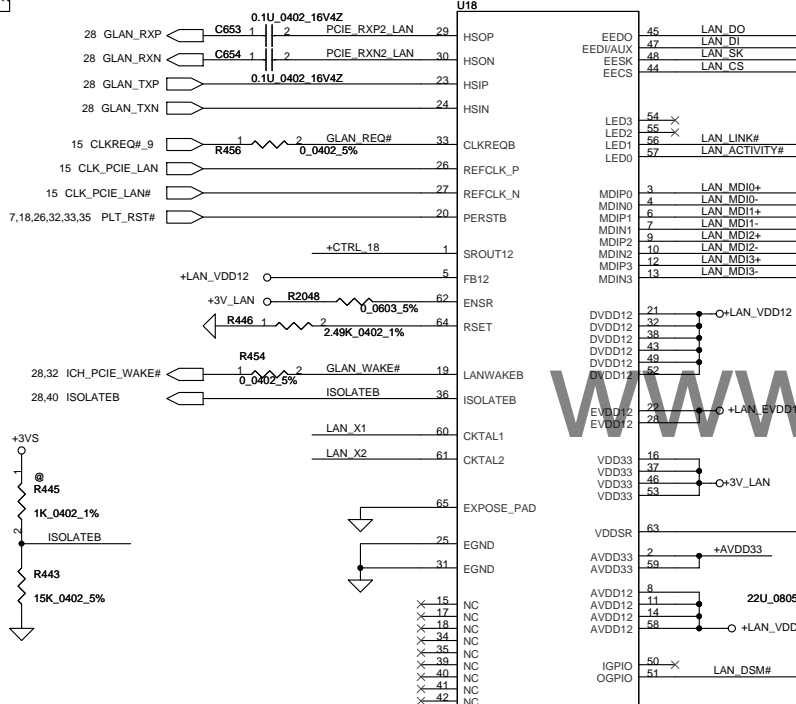
SCHEMATICS, MB A4083

1025 add to meet HP request

The diagram illustrates a circuit modification labeled "1025 add to meet HP request". It features a +3V_LAN input connected to a resistor R1106 (0_1206_5%). The other end of R1106 is connected to a +3VALW input and the gate of a MOSFET Q106 (AP2305GN). The source of Q106 is connected to ground (0V) and the drain is connected to a 40 LANPWR# output. A 10k resistor is connected between the gate and drain of Q106.

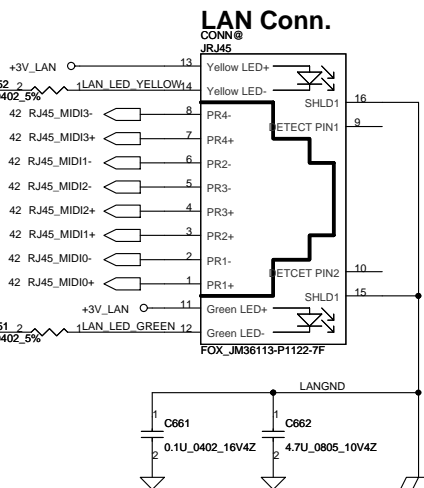
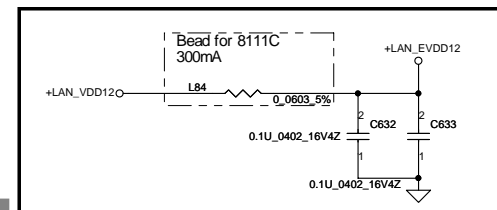
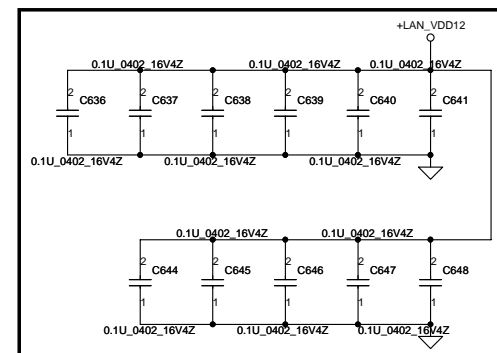
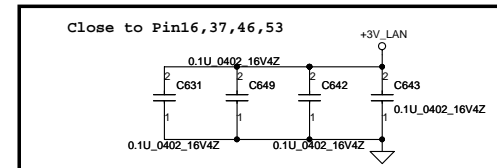
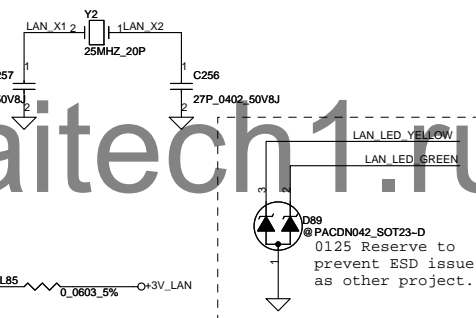
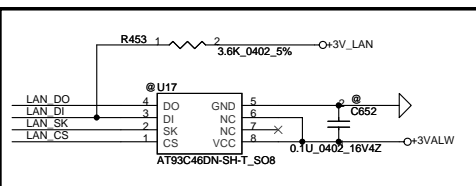
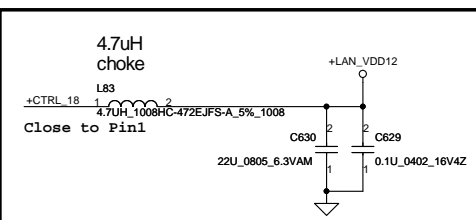
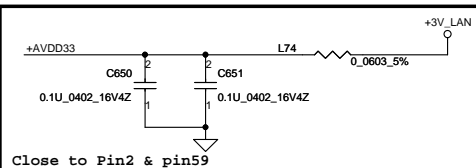


CLKREQ# 9



0.01U_0402_16V7K 0.01U_0402_16V7K 0.01U_0402_16V7K 0.01U_0402_16V7K

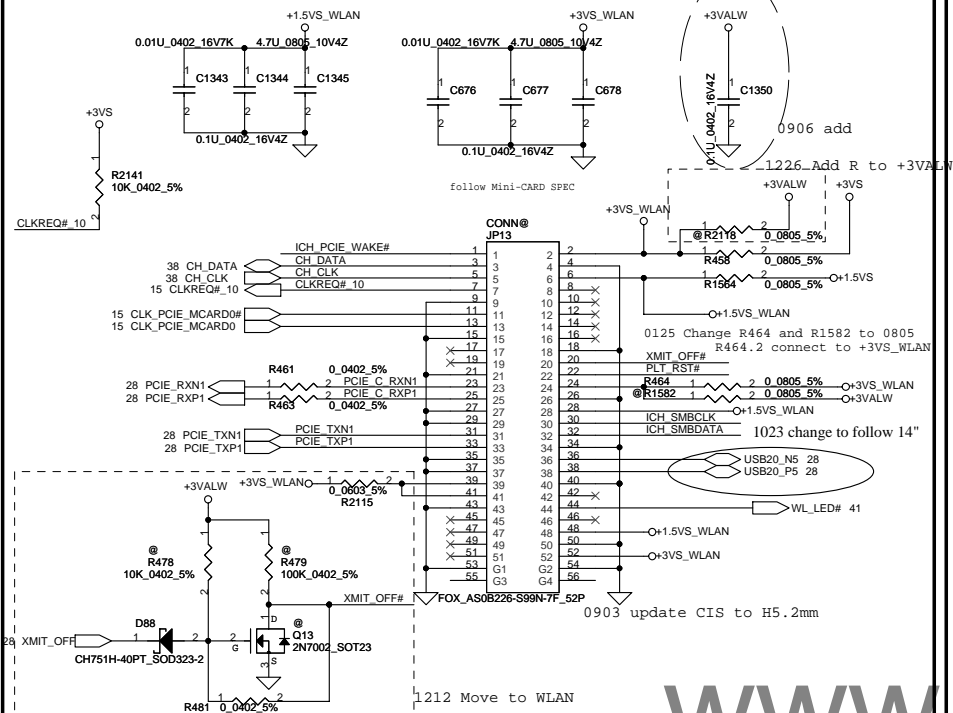
**Place these components
colsed to LAN chip**



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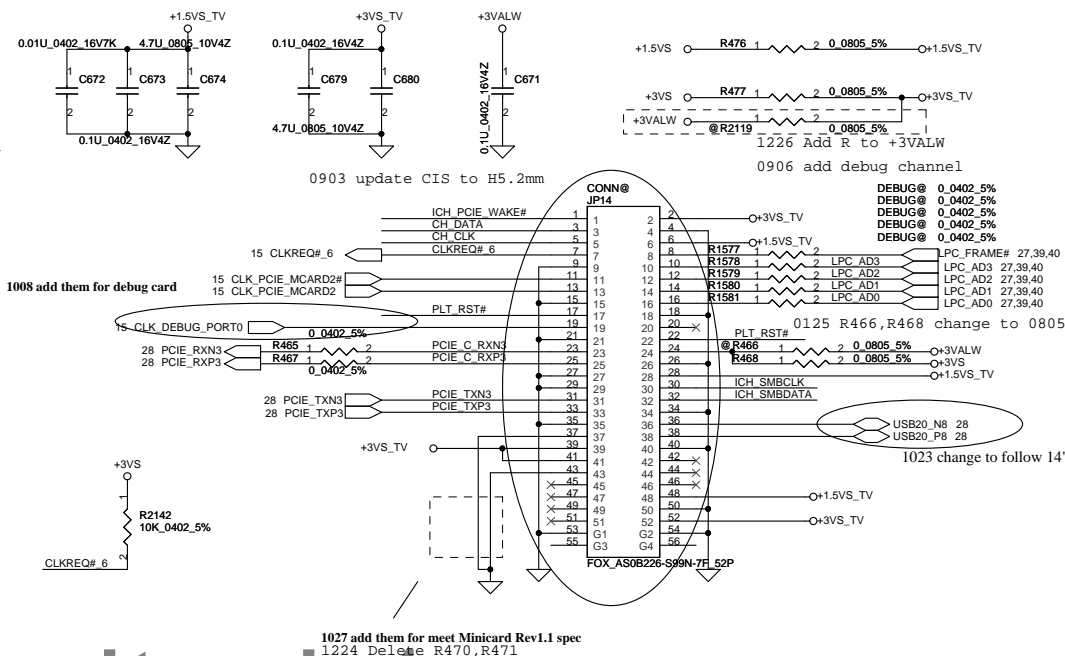
Mini Card 0--WLAN

1022 change to follow HP design



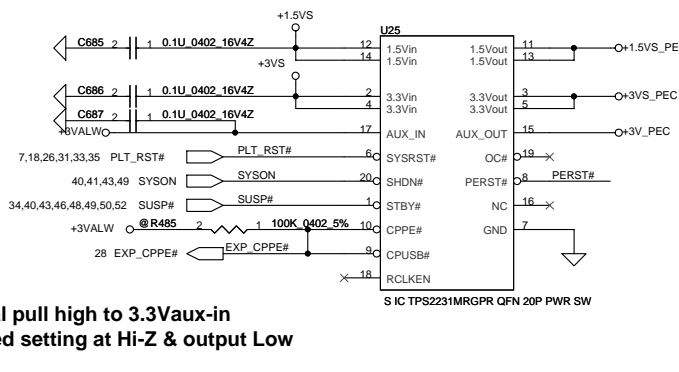
Mini Card 2---TV tuner

1022 change to follow HP design

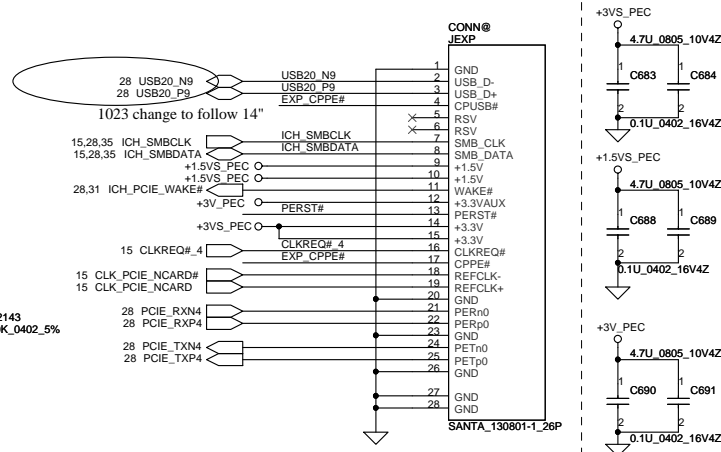


New Card

internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low

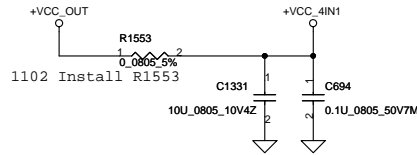


Near to Express Card slot.

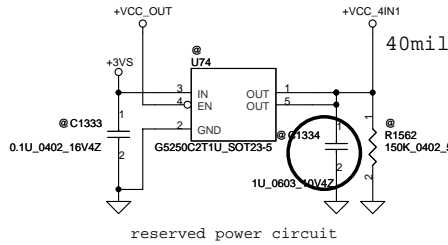


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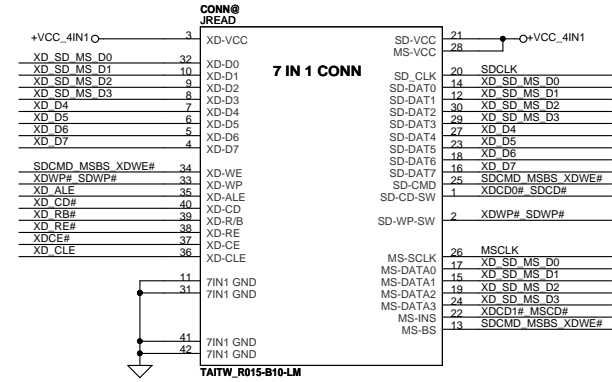
Use 0603 type and over 20 mils
trace width on both side

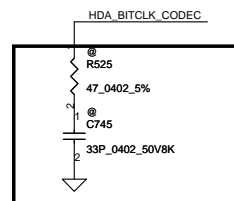
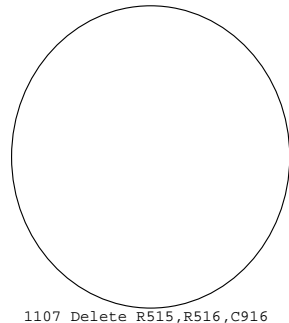
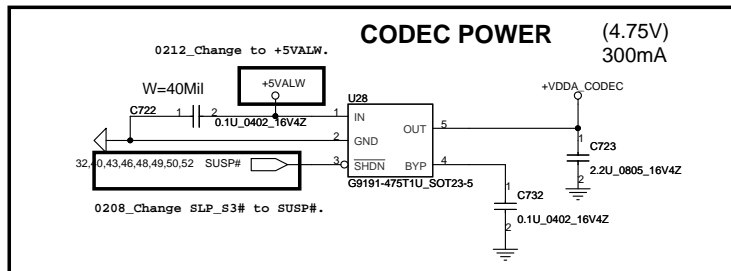


need change to low active switch



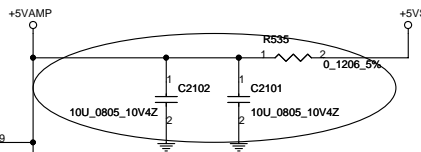
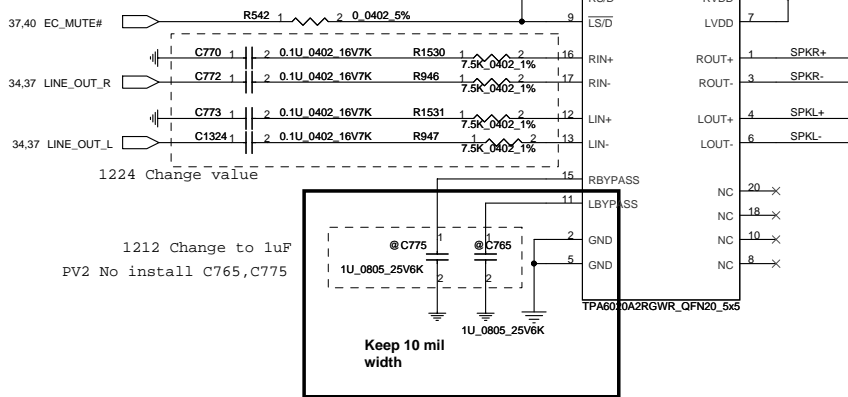
Card Reader Connector



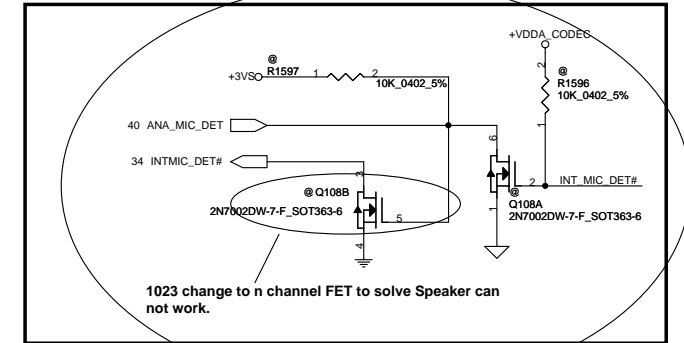
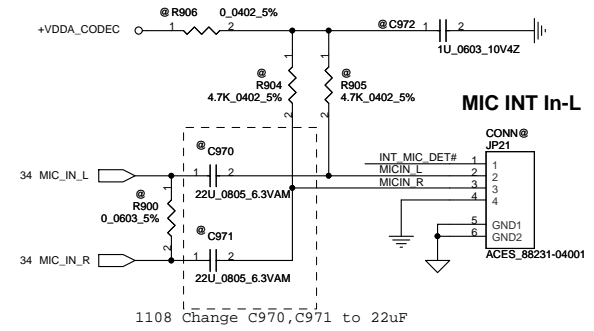
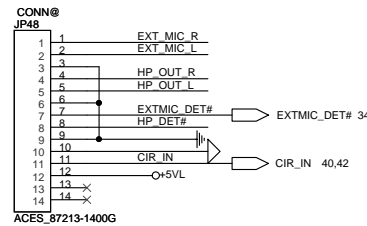


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0906 Change
3/28 from
NC7SZ04P5X_SC70-5
change to 2N7002

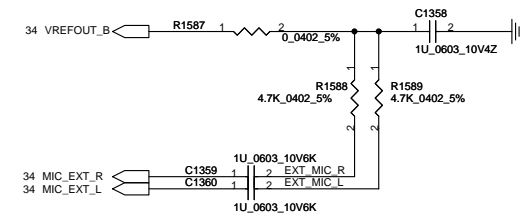
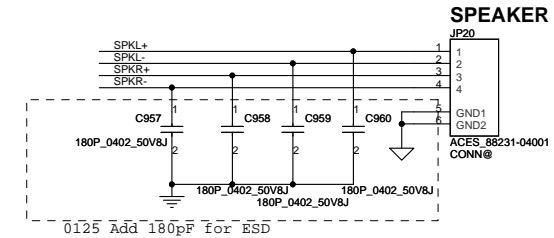
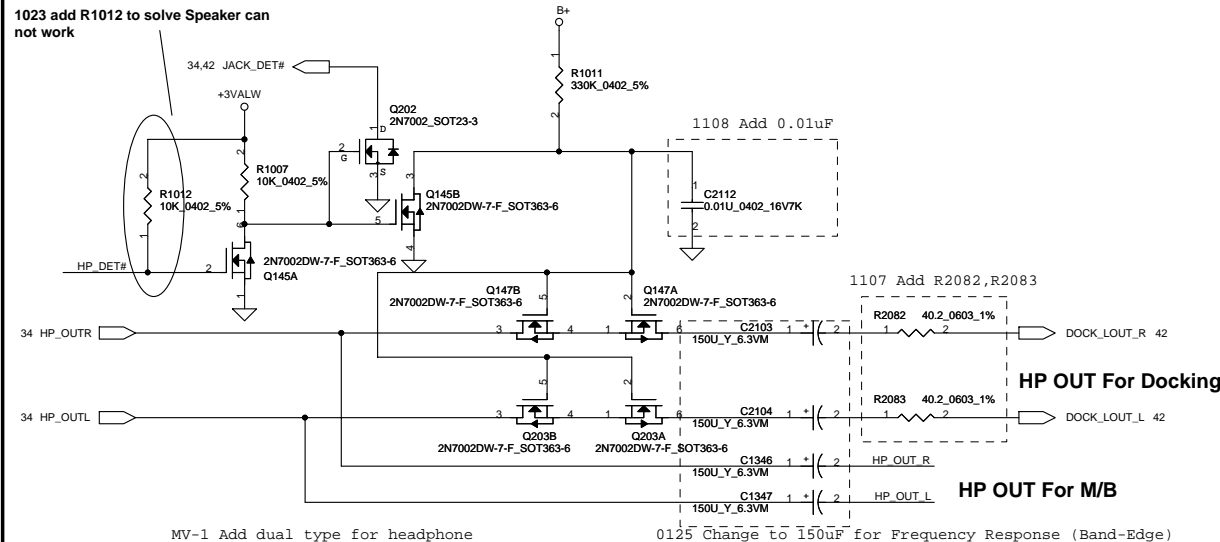


0906 Change pin define
Audio & USB board conn

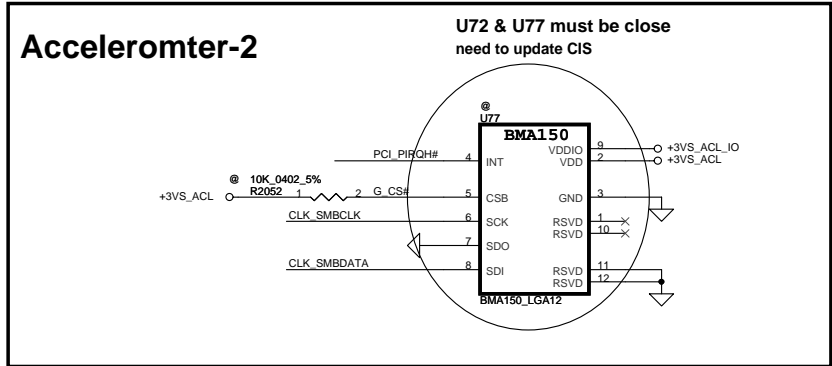
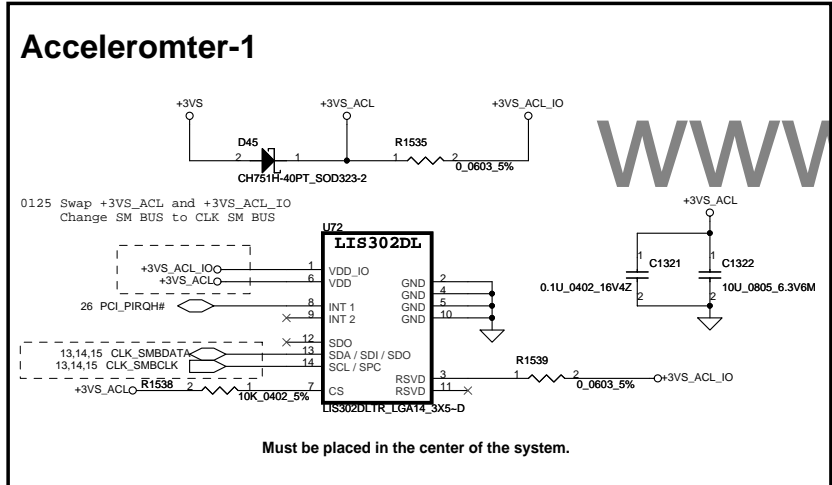
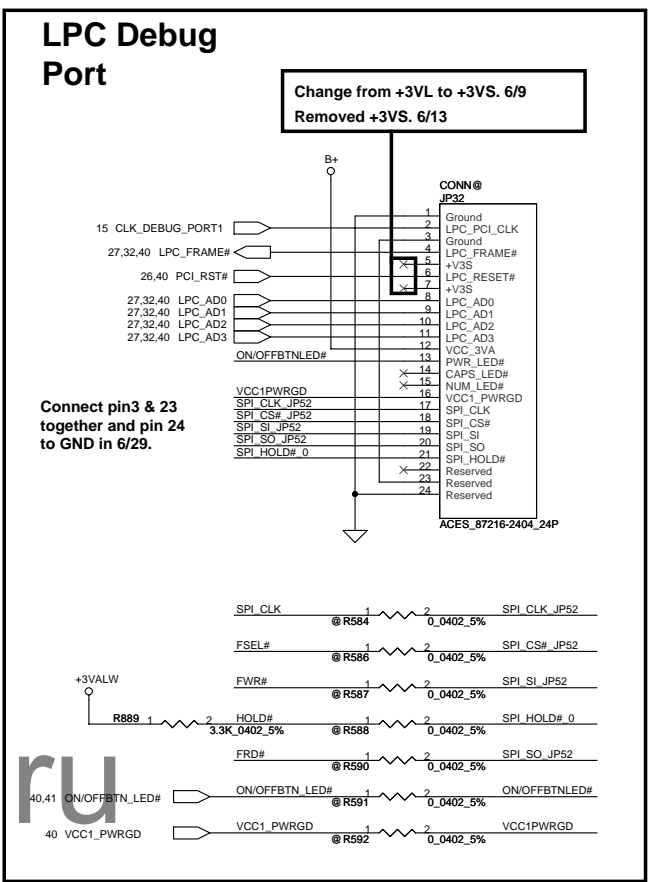
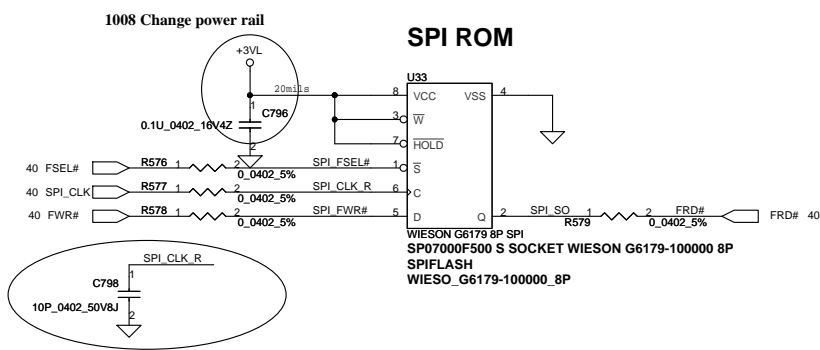
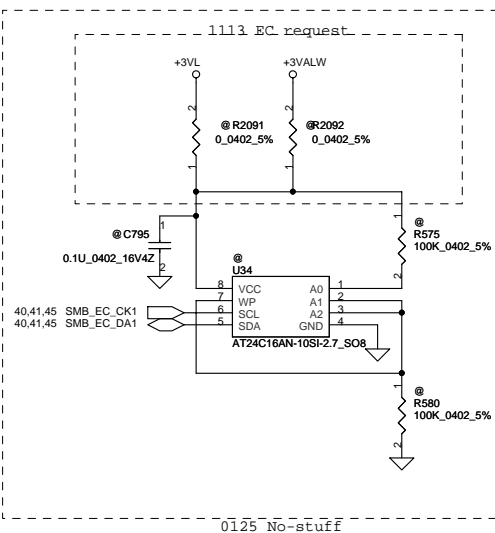


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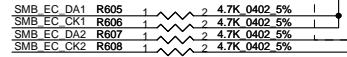
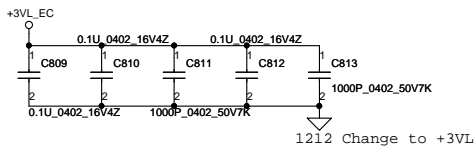
1023 add R1012 to solve Speaker can not work



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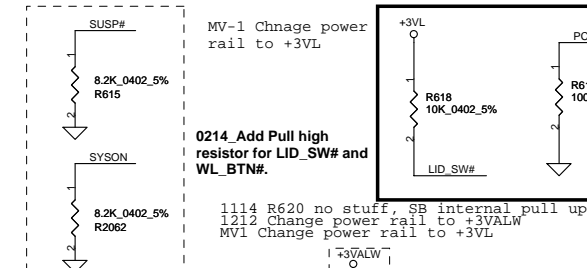
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1025 Add Pull up for GPI

0205 Add Pull down R402 for SUSP#.

1102 Change R615 to 8.2k ohm add pull down on SYSON

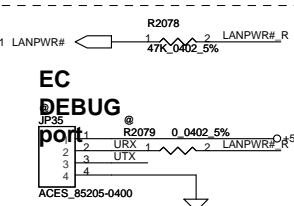


0214 Add Pull high resistor for LID_SW# and WL_BTN#.

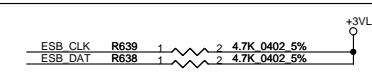
1114 R620 no stuff, SB internal pull up
1212 Change power rail to +3VALW
MV1 Change power rail to +3VL



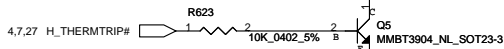
1106 Change LANPWR to KBC pin31



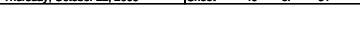
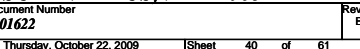
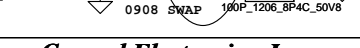
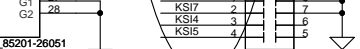
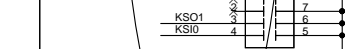
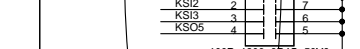
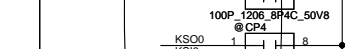
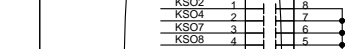
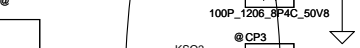
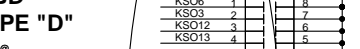
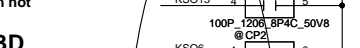
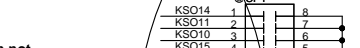
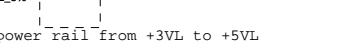
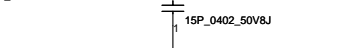
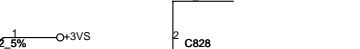
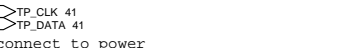
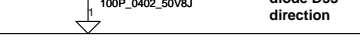
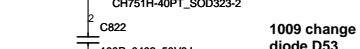
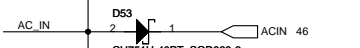
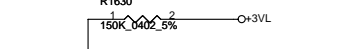
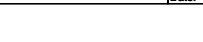
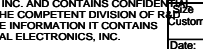
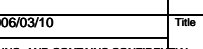
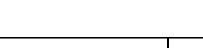
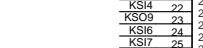
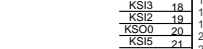
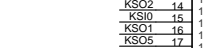
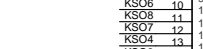
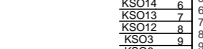
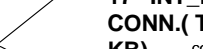
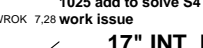
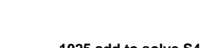
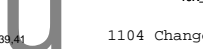
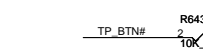
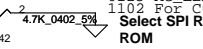
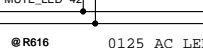
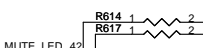
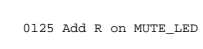
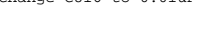
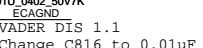
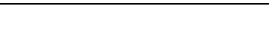
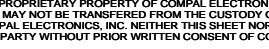
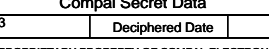
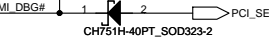
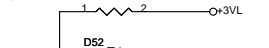
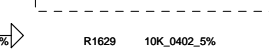
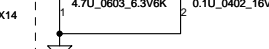
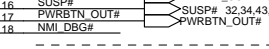
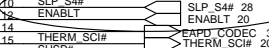
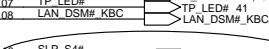
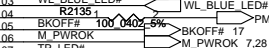
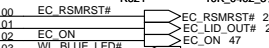
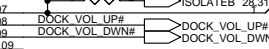
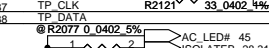
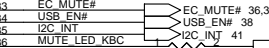
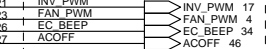
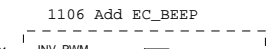
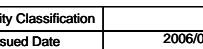
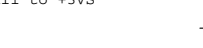
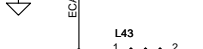
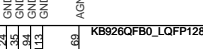
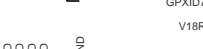
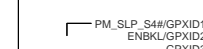
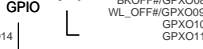
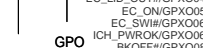
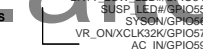
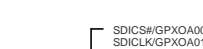
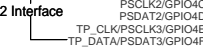
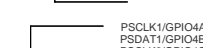
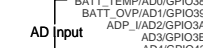
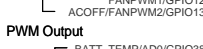
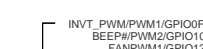
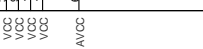
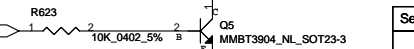
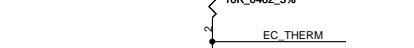
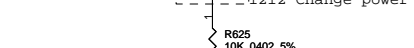
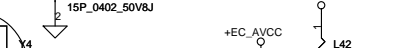
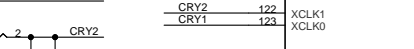
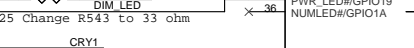
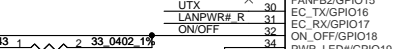
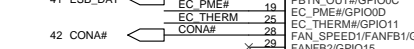
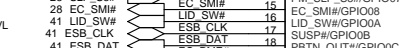
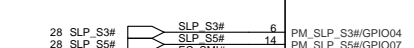
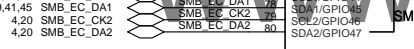
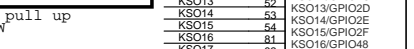
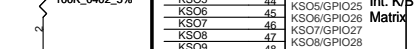
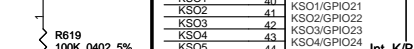
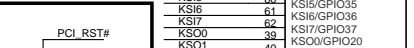
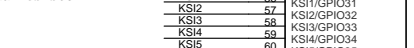
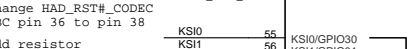
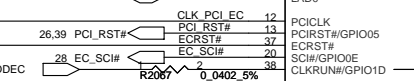
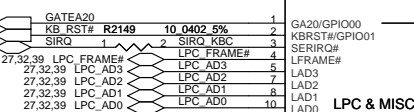
EC DEBUG port



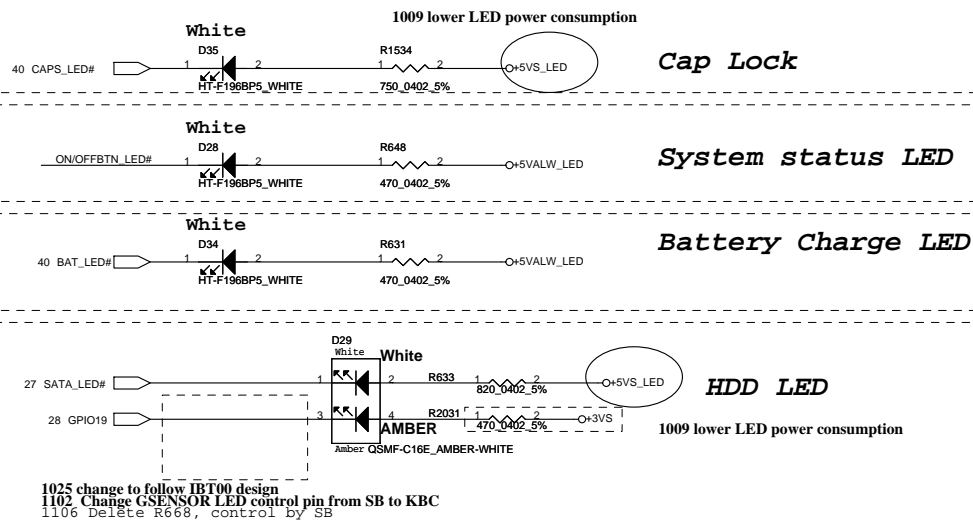
1025 Add Pull up for ESB channel



20080812 Add R2148 for 2F issue

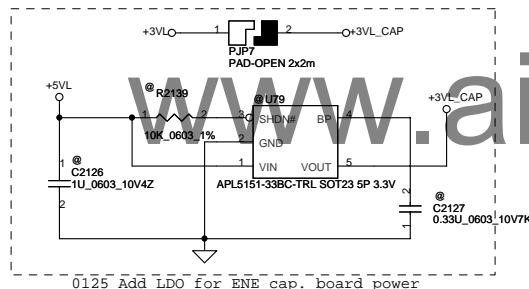


LED

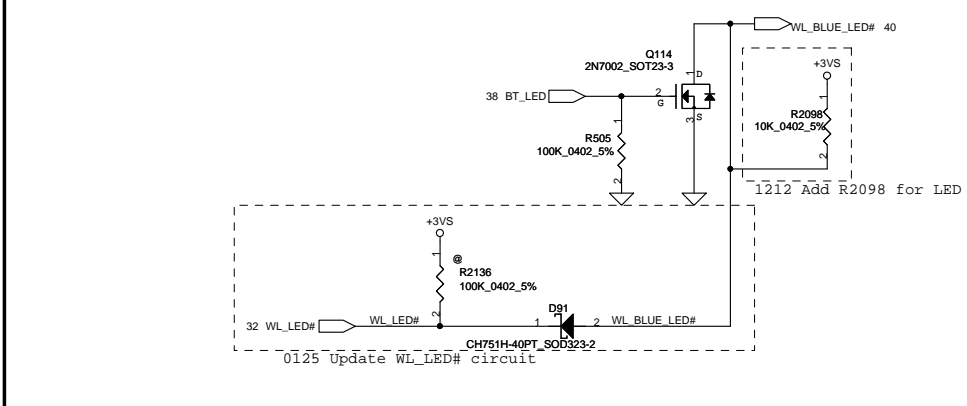
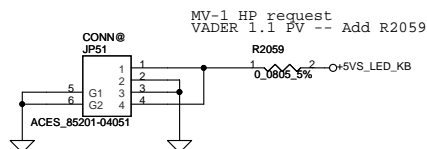


for debug only

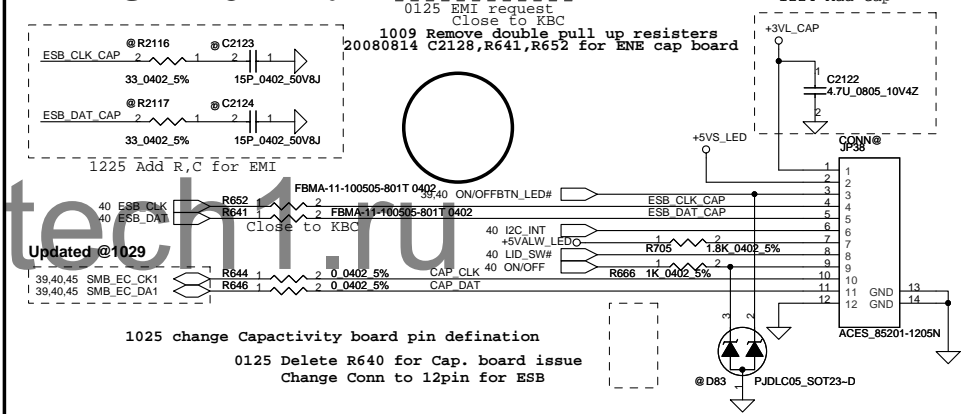
1212 Delete SW5,SW6



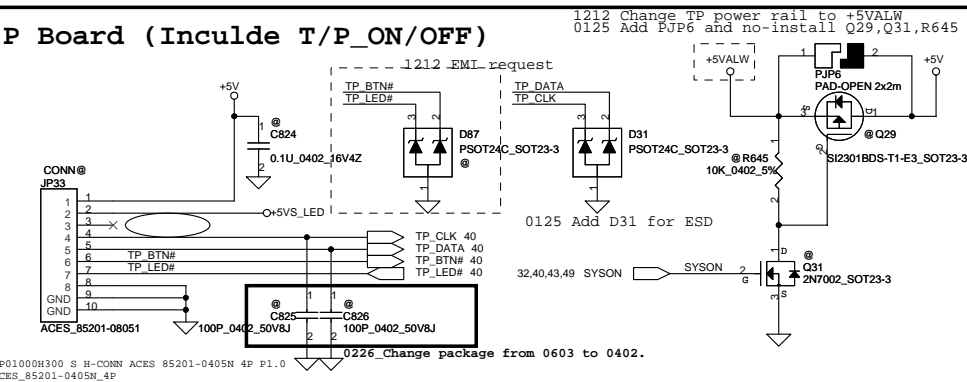
K/B backlight



SWITCH BOARD.

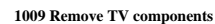
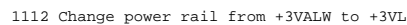


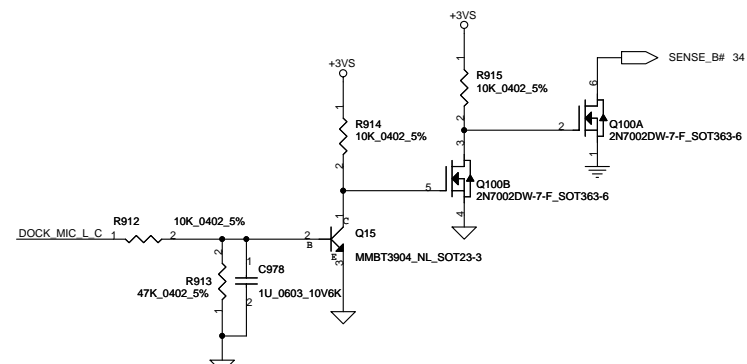
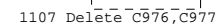
T/P Board (Inculde T/P_ON/OFF)



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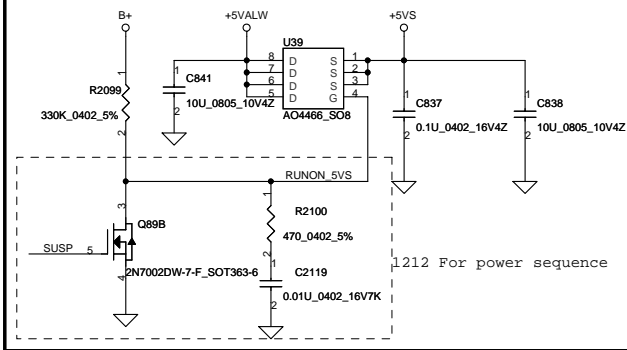
4V = Notebook S0, Dock on



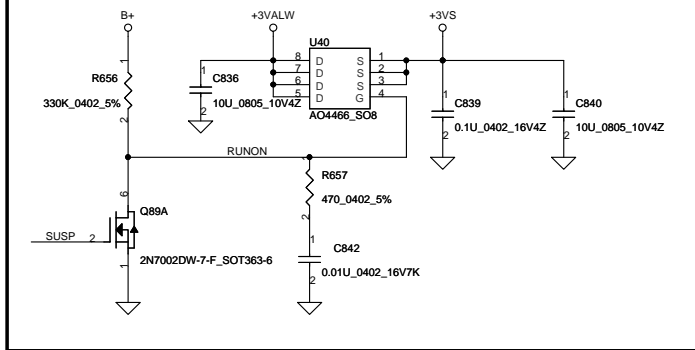


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										Customer									
										Date:		Thursday, October 22, 2009				Sheet		42 of 61	

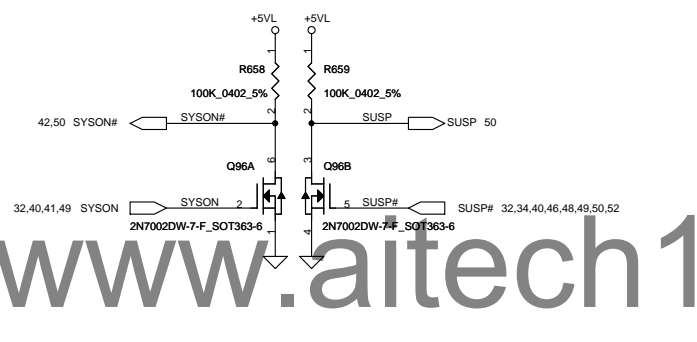
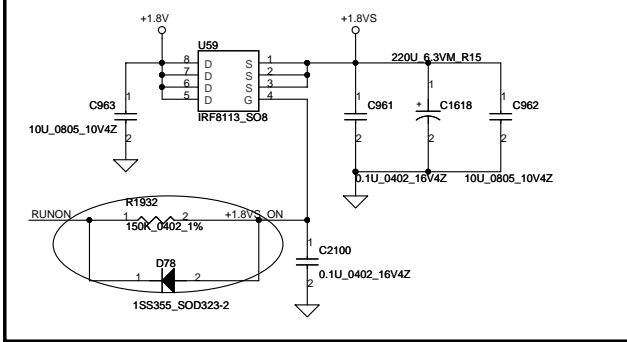
+5VALW to +5VS Transfer



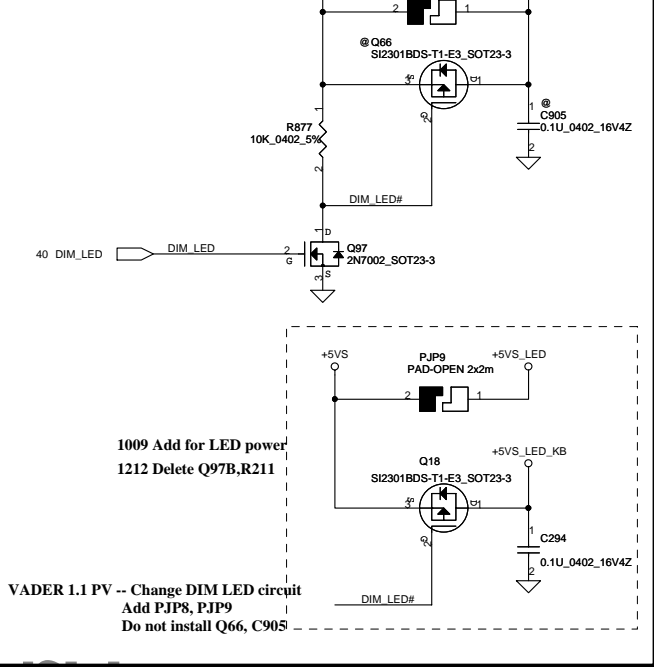
+3VALW to +3VS Transfer



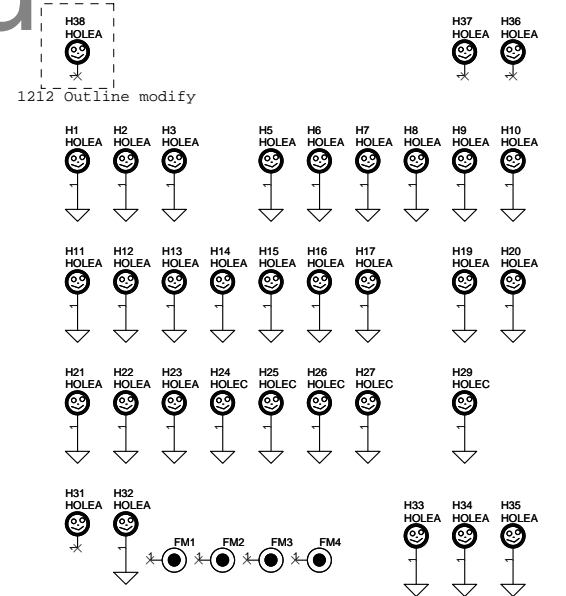
+1.8V to +1.8VS Transfer



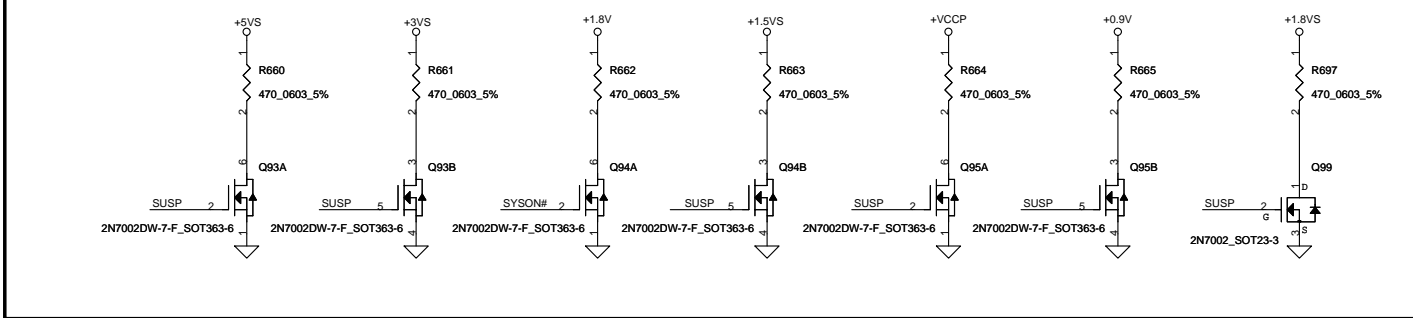
DIMM LED



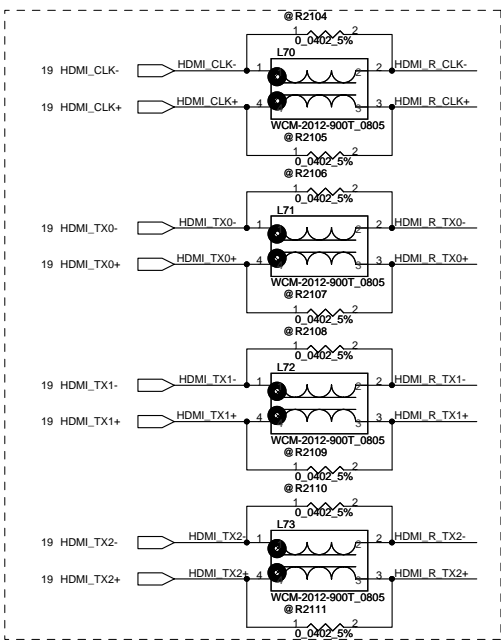
VADER 1.1 PV -- Change DIM LED circuit
Add PJP8, PJP9
Do not install Q66, C905



Discharge circuit

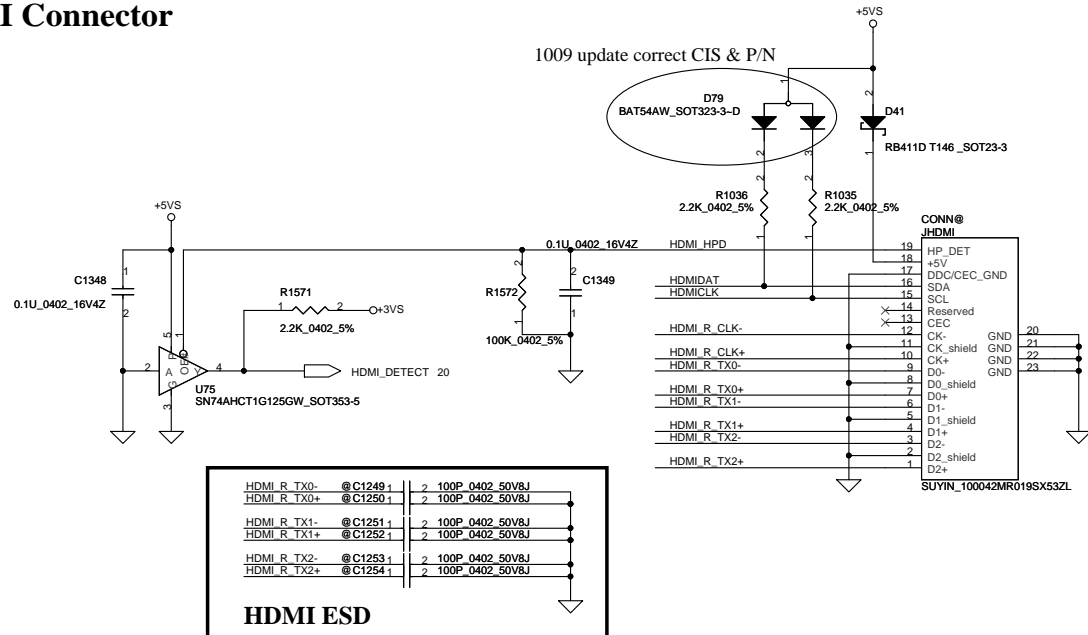


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				401622	E
				Date: Thursday, October 22, 2009	Sheet 43 of 61

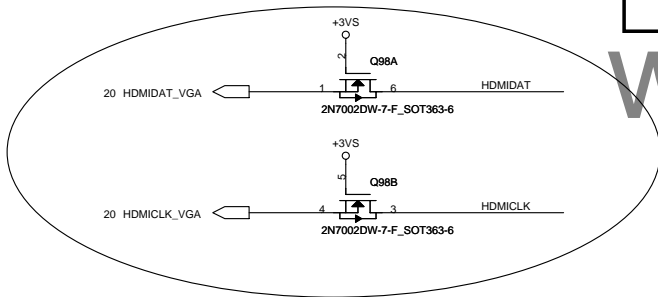


1212 Add 0 ohm

HDMI Connector



www.aitech1.ru

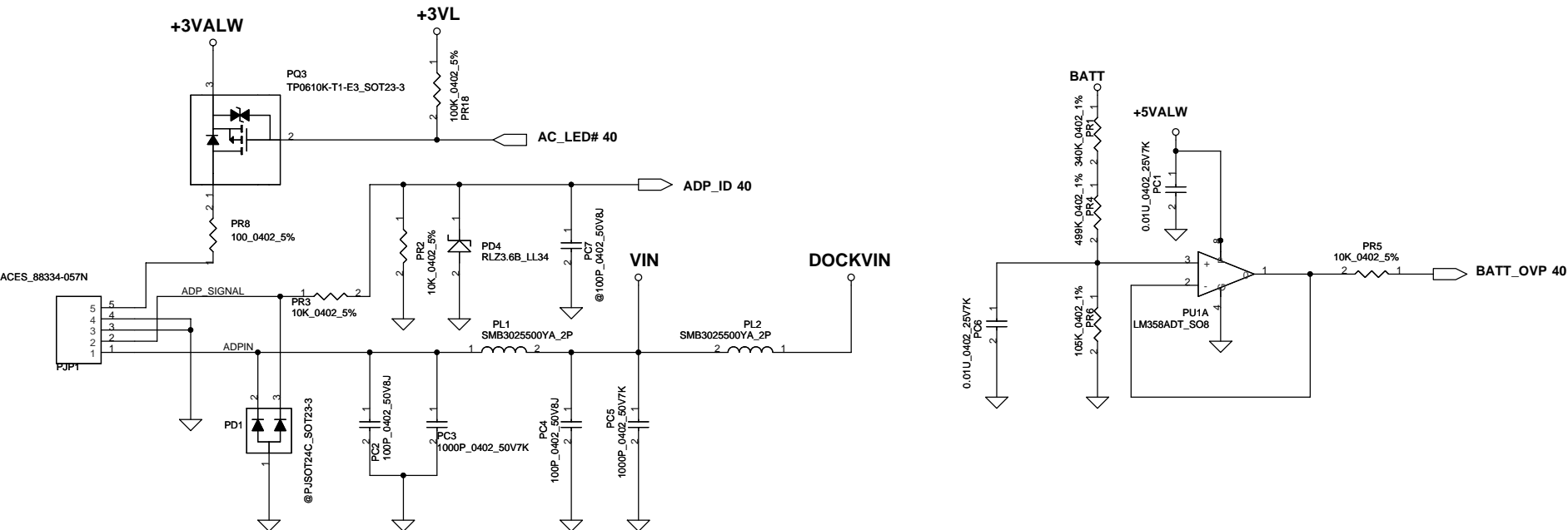


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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Document Number	401622
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				Sheet	44 of 61

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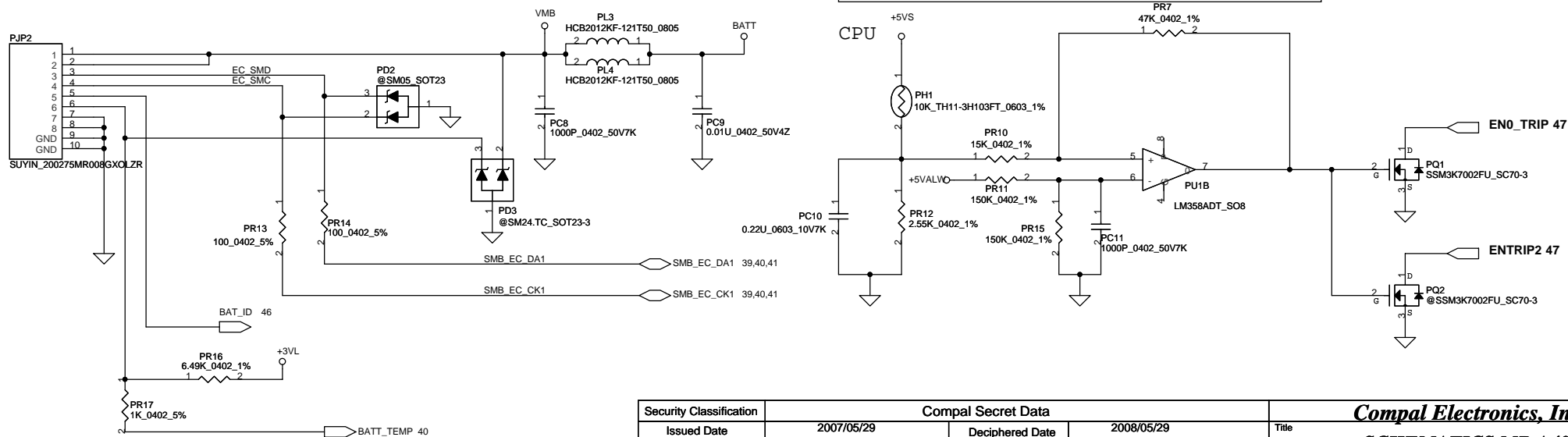
SCHMATICS,MB A4083

Rev E

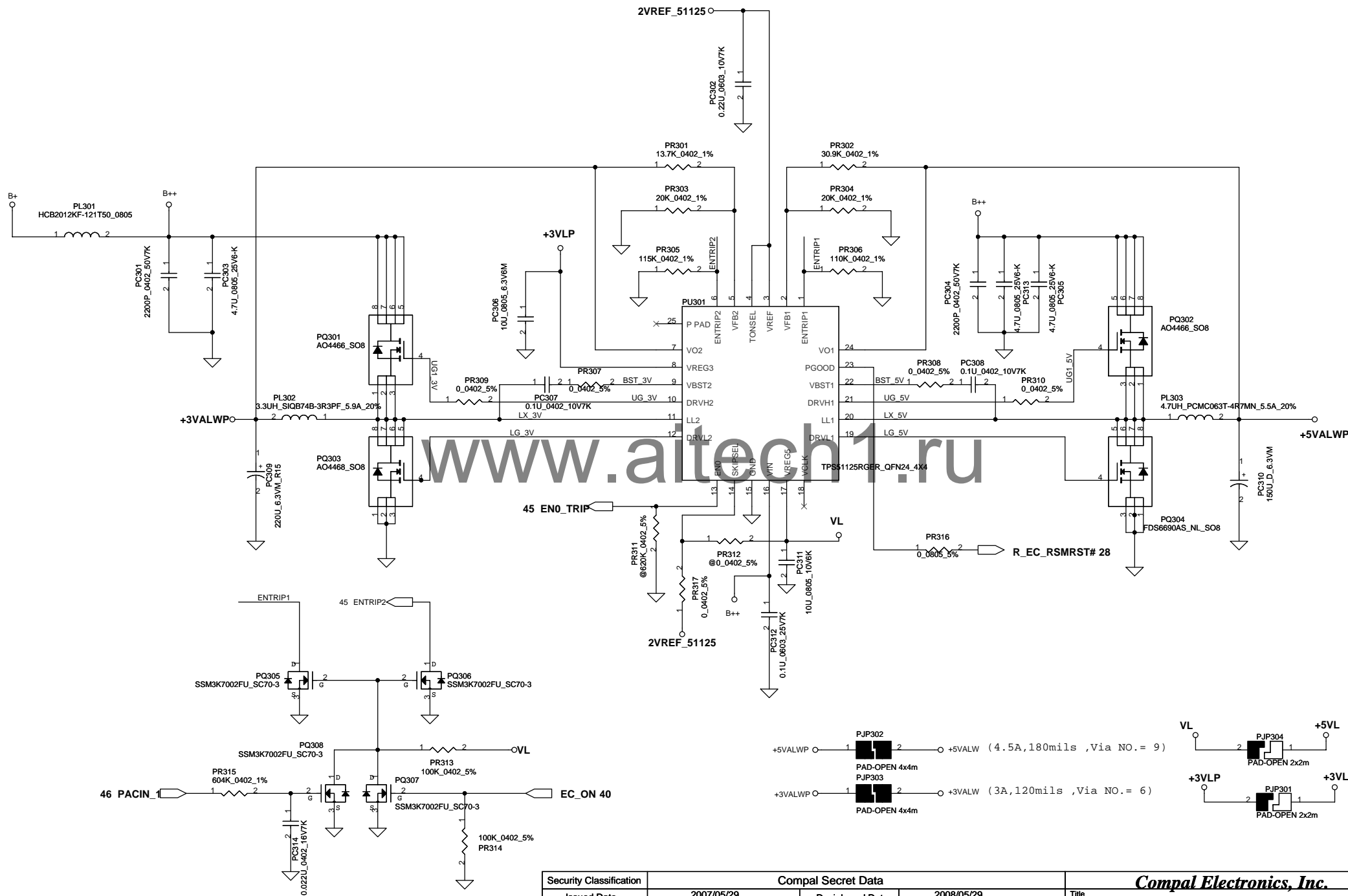


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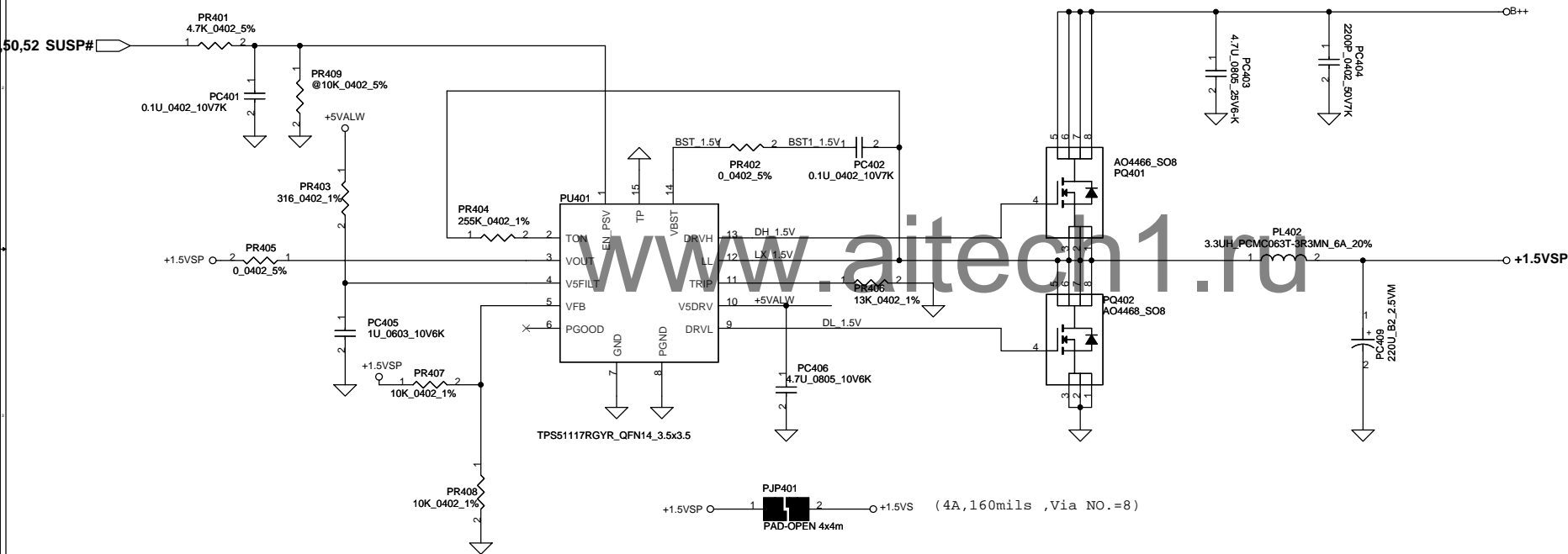
PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C
Recovery at 47 +/-3 degree C



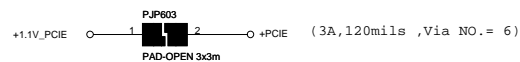
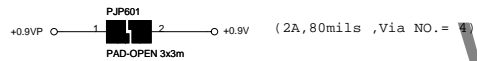
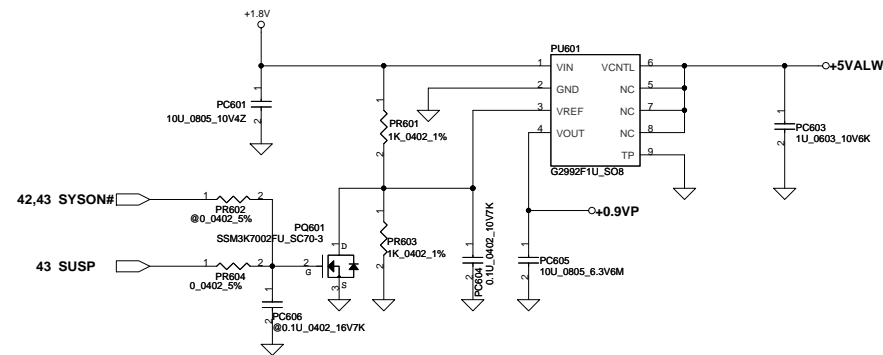
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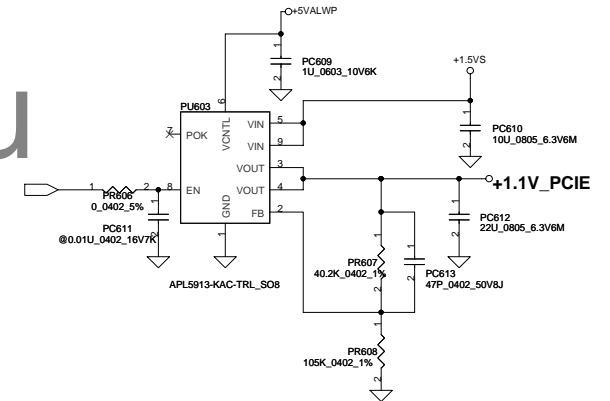
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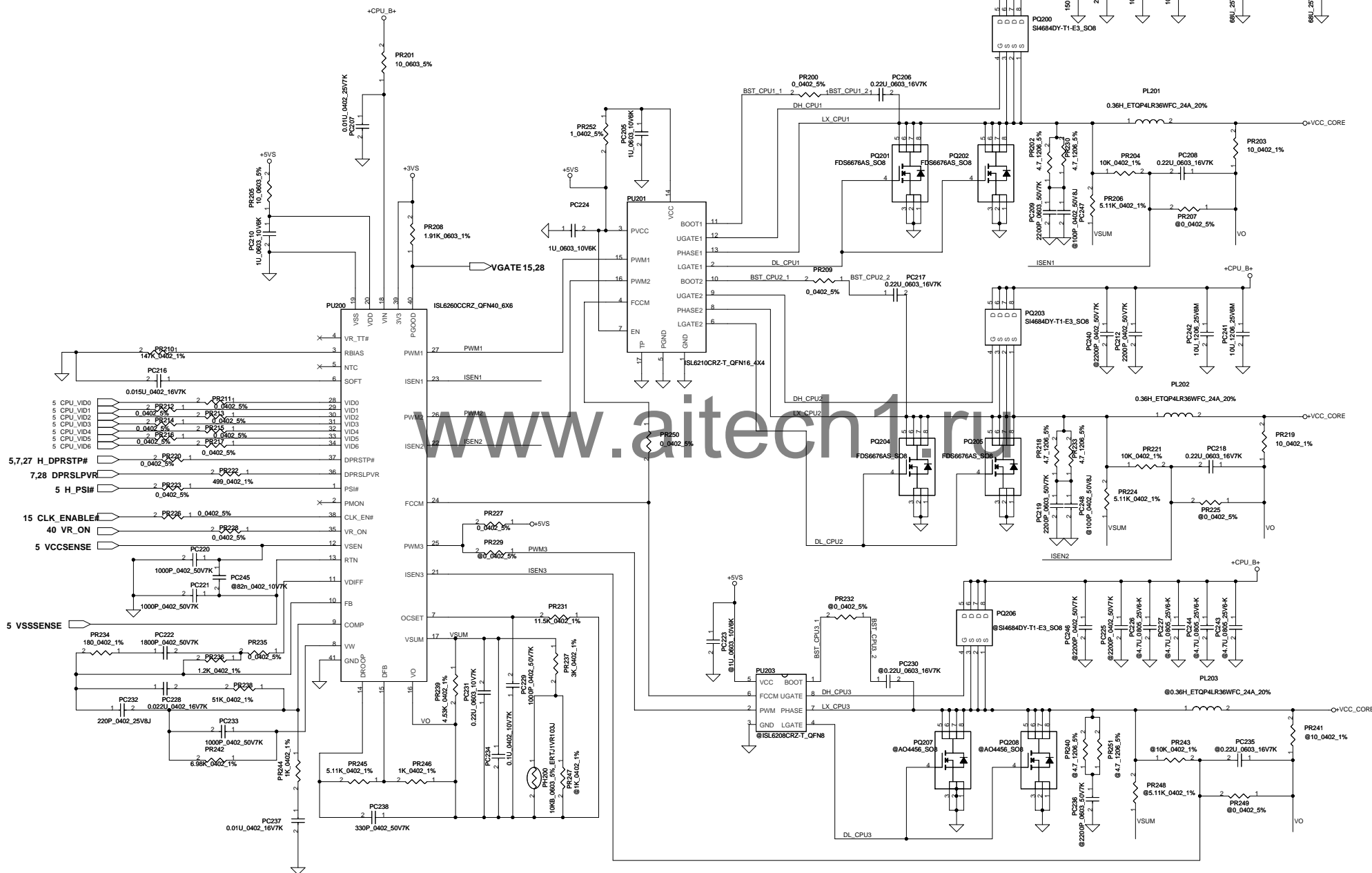
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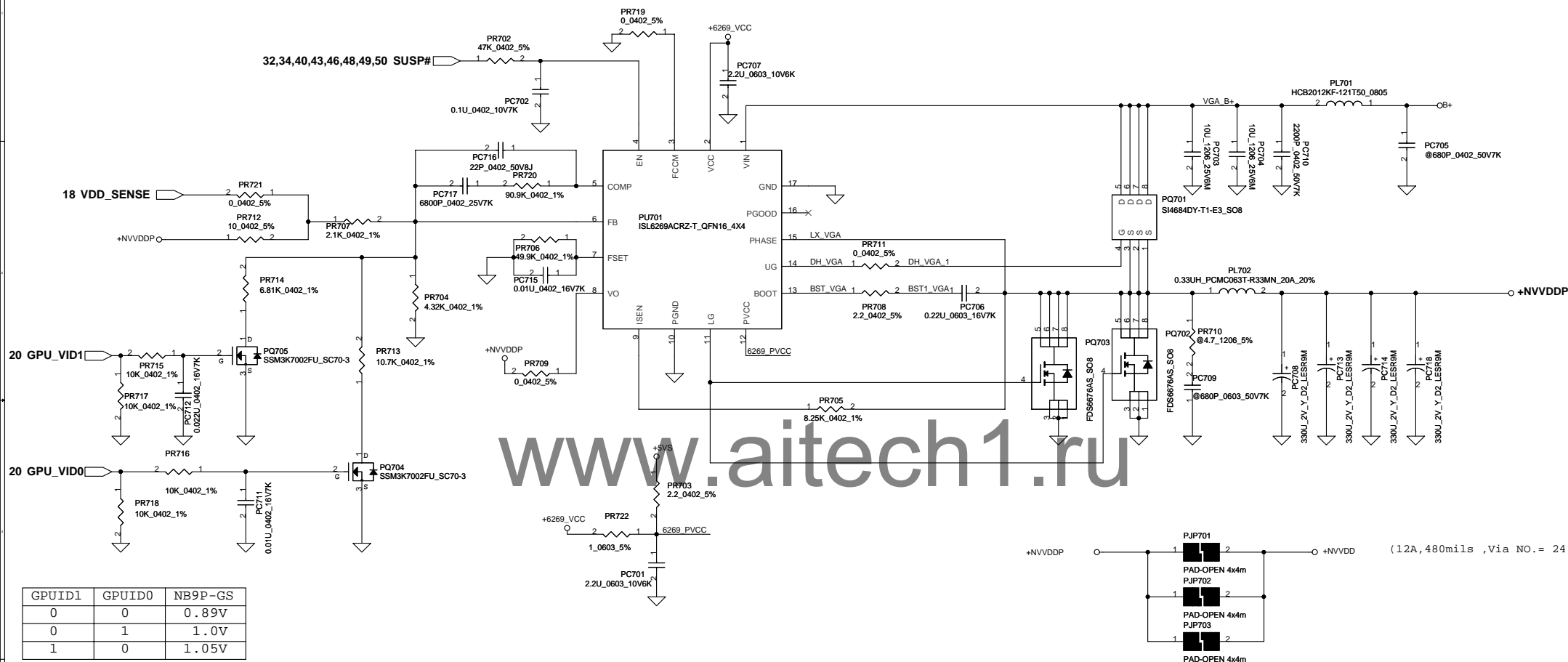


32,34,40,43,46,48,49,52 SUSP#



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GPUID1	GPUID0	NB9P-GS
0	0	0.89V
0	1	1.0V
1	0	1.05V

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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Cut in
1	43 44 50	DCIN/ BATTERY CONN Charger ADP_OCP	2006/09/07	HP R.L.	Change charger control from HW to FW	All the related components	DB1B
2	50	ADP_OCP	2006/10/12	HP R.L.	Identify 65W adapter as "light"	Change PR223 from 180K to 147K	DB2
3	51	VDD_CORE /PCIE_VDD	2006/10/12	HP R.L.	Change VGA chipset from ATi M62S to M64S	Change PR355 from 11K to 9.76K Change PR392 from 33.2K to 24.9K	DB2
4	52	+1.25VMP/ +1.05V_VCCP	2006/10/12	HW Tony J	For HW's requirement, fine tune +1.05V_VCCP sequence	Change PR249 from 0 to 47K Add PC186 as 47pF Install PD45	DB2
5	51	VDD_CORE /PCIE_VDD	2006/10/12	PWR Francis H	Fine tune PCIE_VDD	Change PR358 from 47K to 49.9K Change PR359 from 150K to 100K	DB2
6	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the GPU "Power Play" sequence	Add PC196 as 1uf	SI
8	51	VDD_CORE /PCIE_VDD	2006/11/08	HW Tony J	Fine tune the power sequence of PCIE_VDD	Change PU31 pin5, 9 source from VDD_MEM18 to +1.8V	SI
9	44	Charger	2006/11/08	PWR Francis H	Base on "Energy STAR" spec, reduce S5 and S3 power consumption (AC mode)	Uninstall PQ11	SI
10	48	1.8V/0.9V	2006/11/08	HP	Add PM_SLP_M# sequence	Add PR387	SI
11	52	+1.25VMP/ +1.05V_VCCP	2006/11/20	HW Tony J	For HW's requirement, fine tune +2.5VS sequence	Change PR243 to 47K, Change PC170 to 0.1uF	SI
12	52	+1.25VMP/ +1.05V_VCCP	2007/2/28	HW Tony J	Fine tune the +2.5VS power level to 2.57V (typ)	Change PR244 from 13K to 13.7K	SI2
13	50	ADP_OCP	2007/2/28	HP R.L.	System identity	Change PR223 from 147K to 137K	SI2

	Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2007.10.08>	1	Fix Audio disappear	follow Intel SB design suggestion to separate HDA Bus	27	Add R439, R440, R442, R444	0.2
	2		Add to determine board type and project	28	Add R777, R776, R774, R775	0.2
			Meet EC request	28	non-stuff R419, R695	
	3	Fix Audio disappear	follow Intel SB design suggestion	29	Change power rail from +1.5v to +3v	0.2
	4		meet SW debug request	32	Add Debug CLK and PLT_RST#	0.2
	5	Fix Audio disappear	follow Intel HDA bus design for Discrete platform	34	Change codec power rail from +1.5v to +3v	0.2
	6	Fix can not power on issue	Meet EC and SPI access sequence	39	change SPI power rail from+3valw to +3VL	0.2
<2007.10.09>	7		Follow Intel design guide	7	Change R30 value	0.2
	1	Fix HDMI can not detect	follow Nvidia design request	18	change HDMI I2C channel to I2C B channel	0.2
	2		Meet HP request to remove TV	18	Remove TV all components at VGA side	0.2
	3		update ODD footprint	30	update JODD footprint	0.2
	4	Fix ODD wrong pins	lower system power consumption	33	change Card Reader LED power rail	0.2
	5		Meet Sub-woofer pwoer request	37	change D81, D82	0.2
	6	Solve EC always damage	Solve EC always damage	40	change D53 direction	0.2
	7		Double pull up and pwoer rail is different	41	Remove pull up resistors	0.2
	8		lower system power consumption	41	change Cap-lock, HDD LED power rail	0.2
	9		Meet HP request to remove TV	42	Remove TV all components at Dock side	0.2
	10		lower system power consumption and meet LED status	43	Add +5VS_LED (Inculde DIM function)	0.2
<2007.10.19>	11		solve HDMI pull up	44	update D79 footprint	0.2
	1		Meet ME limit area at KBC	27	Change Y4 material	0.2
	2		Follow IDT suugestion	35	change R886 to 1206	0.2
<2007.10.20>	3		Follow Nvidia suggestion	25	Change R193, R196 size to 0603	0.2
	1		follow correct power rail	38	change Touch screen power rail	0.2
	2		Meet HP request	39	Change ST G-sensor P/N & package	0.2
<2007.10.22>	3		Meet HP request for WLAN &TV slot swap	32	Swapped WLAN and TV all support components	0.2
	1		Change LAN chip to meet Energy star spec	31	change LAN brand to Realtek	0.2
	2					

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		5	4	3	2	1		
		Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.	
<2007.10.23>	1	Fix USB loading of SB	follow 14" Blade USB channel design	28	Chnage all USB channel	0.2		
				17	Change USB channel of Camera			
				32	Change USB channel of WLAN & TV Tuner & New card			
				38	Change USB channel of Left side, Right side, E-SATA			
				38	Change USB channel of Touch screen, Finger print			
				42	Change USB channel of Dock			
	2		Follow JMicro CardReader Vendor Suggestion	33	Change R114 & R1546 value	0.2		
	3		Solve Speak no sound issue	36	add pullup at HP_DET#			
				36	Change Q203 to N-channel FET	0.2		
				34	Change R524 pin2 connect to JACK_DET#			
<2007.10.25>	1		Meet HP request for QC and DC co-lay	4	add GTLREF and XDP circuits			
				5		0.2		
				6				
	2		Meet Intel request for CLK request	15	Add R127 to meet Intel CLK design	0.2		
	3		Solve G-sensor LED control	28, 41	change G-sensor LED control to GPIO19 of SB	0.2		
	4		Follow Capactivity board design	41	change Pin7 & 7 NET	0.2		
<2007.10.31>	1			34	Use Audio Codec GPIO5 to shutdown Sub-woofer			
	2			40	Connect HDA_RST#_CODEC to EC			
	3			34	Separate SPDIF out to VGA and Docking			
<2007.11.02>	1		Common design	16	R204,R205 no stuff	0.3		
	2		Change +5VS_LOGO resistor size to 0805	17	R642 size to 0805	0.3		
	3		Double pull up	20	R2046,R2047 no stuff	0.3		
	4		For card reader power	33	install R1553	0.3		
	5		For KBC C0 version	40	R616 no stuff	0.3		
	6		Add pull down resistor for SUSP# and SYSON	40	Change R615 to 8.2k and add R2062	0.3		
	7		Change HAD_RST#_CODEC from KBC pin 36 to pin 38	40		0.3		
	8		Change GSENSOR LED control pin from SB to KBC	41	Install R668, no install R667	0.3		
	9		Add pull down for sub-woofer power-down	37	Add R2063	0.3		

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
<2007.11.04>	1	Move resistor from LS4086P to MB	41	Add R2064	0.3
	2	Change to dual type for layout space	16	Change Q69,Q70 to dual type	0.3
	3	Only use LIS302DLTR	39	U77, R2025 no install	0.3
<2007.11.05>	4	Change CIR_IN power rail	40	Connect R642.1 to +5VL	0.3
	1	nVIDIA suggestion for NB9M-GS/GE	22	R1005 change to 475 ohm	0.3
<2007.11.06>	2	nVIDIA suggestion -- add Pull up 2.2K on HDMIDAT_VGA and HDMICLK_VGA to +3VS. at VGA side	18	Add R2065,R2066	0.3
	1	EMI request	CRT add resistor for EMI	16	Add R2069,R2070,R2071
<2007.11.07>	2	HP suggestion	34	Change C746,C747,C748,C749 to 1000PF	0.3
	3	USB camere power and add GPO pin for shutdown	17	Add PJP5,R2072,R2073	0.3
	4	LAN DSM support	31	1. USB camera - SB GPIO20 2. ISOLATE - SB GPIO18 3. LAN OGPIO - SB GPIO14	0.3
	5	EC_BEEP	34	Add R2076	0.3
	6	G-sensor LED control by SB	41	Delete R668	0.3
	1	Modify FPR connector pin assignment	38	Modify JP41 pin assignment	0.3
<2007.11.08>	2	Modify Audio	34 36 37 42	1. Add C2108,C2109,R2080,R2081 2. Add R2082,R2083 3. Change C1008,C1009 to 1UF 4. Delete C976,C977 5. Delete R515,R516,C916 6. Change C982,C980,C984 from 5900p to 0.039u 7. Change C983,C992 from 1000p to 100p 8. Add EC_MUTE# to sub-woofer shutdown pin and R2084	0.3
	3	nVIDIA suggestion	20	1. Delete strap pin 2. Change R1020, R1015, R1010 to 475 ohm 3. Swap THERMDN and THERMDP	0.3
	1	EMI request	17	Add C2100,C2111	0.3
<2007.11.09>	2	Audio	36 37	Change C970,C971 to 22uF, add C2112, change D38 to dual type	0.3
	1	nVIDIA suggestion	19 20	Change HDMI DDC to I2CD R387,R388,R415,R422,R427 -- install Change R415 to 10 ohm and no install Delete R99, Change +IFPC_PLLVDD to +PCIE	0.3
<2007.11.12>	2	JMicron suggestion	33	Do not install R2030 Add D86 for card reader wake up Add SB GPIO22 for wake up event	0.3
	1	HP request	4	Add EMC1403 for Qaud core	0.3

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<2007.12.12>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		MV DG for VDDC_QDAC	10	Chagne VCCD_QDAC to +1.5VS	0.4
2		WLAN issue	32	Change XMIT_OFF#,WL_LED# and component to WLAN connector	0.4
3		PCIE issue	28	Swap GLAN and NewCard PCIE port	0.4
4		Modify CardReader LED	33	Use 2N7002 to control LED	0.4
5		KBC	40	Change SMB_EC_DA1,SMB_EC_CK1 power rail from +5VL to +3VL Add C2118 for KBC pin124 Chagne EC_THERM power rail to +3VS	0.4
6		WL_BLUE_LED# issue	41	Add R2089 pull up for WL_BLUE_LED#	0.4
7		Power sequence	43	Add R2099,R2100,C2119 and Q89 change to dual type	0.4
8		DIM_LED	43	Delete Q97B,R211	0.4
9		EC_PME#	40	Change EC_PME# power rail to +3VALW	0.4
10		WLAN issue	28	Add R2101	0.4
11		Change TP power rail	41	Change TP power rail to +5VALW	0.4
12		G-sensor	41	G-sensor -- R2031 change to 470 ohm and pull up to +3VS	0.4
13		For Dock present	42	R1570 change to 22 ohm,R61 change to 2K ohm	0.4
14		Clock generator	15	Add series R2102,R2103 for 27M_SSC and 27M_CLK	0.4
15		HDCP ROM	19	R951 pull up,R959 no install	0.4
16		EMI request	17	C272,C273,C2120 -- 470pF C828,C798 -- 10pF C2111 -- 220pF Add D87	0.4
17		Modify BT/FPR circuit	38		0.4
<2007.12.24> 1		HP request	36 37	Change value	0.4
<2007.12.25> 1		For ENE cap board EMI issue	40	Add R and C	0.4
<2007.12.26> 1		For Mini PCI	32 35	Add R2118,R2119,R2120	0.4

<2008.01.25>

Item	Fixed Issue	Reason for change	PAGE	Modify List	M.B. Ver.
1		G-sensor power rail G-sensor SM BUS	39	Swap +3VS_ACL and +3VS_ACL_IO Change G-sensor SM BUS to CLK SM BUS -- +3VS power rail	0.5
2		KBC PIN97 -- AC in LED issue For DOCK_SLP_BTN# For Mute_LED	40	KBC pin 97 connect to power Change R543 to 33 ohm Add R2121 33 ohm	0.5
3		Cap. board INT issue	41	Delete R640 for Cap. board issue	0.5
4		Current issue	32 32 35	Change R464 and R1582 to 0805 R466,R468 change to 0805 R469,R1583 change to 0805	0.5
5		KBC EEprom issue	39	Do not install KBC EE prom	0.5
6		Frequency Response (Band-Edge)	36	Change C2103,C2104,C1346,C1347 to 150uF	0.5
7		D3E function	33	Do not install R2087 for Intel platform	0.5
8		Change BT connector(JP30)	38	Change BT connector from 88231-0800 to 87213-0800(SP02000CZ00)	0.5
9		Audio circuit	37	Change C982 from 0.039u to 5900pF	0.5
10		BKOFF# issue	39	Add R2122 on BKOFF# and no-stuff	0.5
11		TP LED	41	Add PJP6 and no-install Q29,Q31,R645	0.5
12		RTC timing	27	Change C548,C549 to 18PF	0.5
13		Change LED control signal	33	Add R2123 and R2124 No-install R1548,Q53,R2097	0.5
14		Quad Core CPU	4,6	R2125,R2126,R2127,C2125,R2128-R2134	0.5
15		ESD	36 41 38	Add D31 for TP --- OK Change D33 to PRTR5V0U2X_SOT143-4 and install -- Check P/N Add C957,C958,C959,C960 -- 180pF	0.5
16		PM_PWROK timing	28	Add D90 and R2135 for PM_PWROK timing	0.5
17		ENE cap. board	41	Change JP38 to 12pin Change R641,R652 to 800 ohm bead	0.5
18		Reduce 0 ohm		Delete R622, R404, R407, R429, R438, R667, R970	0.5
19		change WLAN LED circuit	41	Need to change R2098 value, Add D91, R2136	0.5
20		ESB LDO CIRCUIT	41	Add U79,R2139,C2126,C2127,PJP7 for ENE cap. board power	0.5
1		nVIDIA suggestion	19	Change R951 and R953 to 2.2K ohm	0.6

<2008.03.16>

[illegible]

